High-Speed On-Chip Signaling: Voltage or Current-Mode?

Riadul Islam

Riadul Islam is with the University of Michigan,
MI 48128 USA (e-mail: riaduli@umich.edu)

October 1, 2018

ABSTRACT

In this paper, we investigate several on-chip signaling schemes. Specifically, we compare different voltage-mode (VM) and current-mode (CM) signaling schemes considering power, performance, and robustness. In addition, we propose a new CM signaling scheme that uses a simple NAND-NOR gate transmitter circuit and a current-comparator-based receiver circuit. We implemented each signaling scheme using a 45nm CMOS technology. The extracted simulation results show that a traditional CM signaling scheme consumes 58–78% less power compared to a traditional buffered VM signaling scheme in the 1–3GHz frequency range. Our proposed CM signaling scheme consumes up to 95% and 81% lower power compared to buffered VM and existing CM schemes, respectively. In addition, the proposed CM signaling scheme has 37–41% lower latency with similar slew-rates compared to the buffered signaling scheme.

Keywords:
Signaling, low-power, current-mode, voltage-mode, interconnect, low-swing.

1. Introduction

The modern central processing unit (CPU) that has defined the performance of a computer for many years is facing several challenges. These bottlenecks can be identified as the memory bottleneck (the bandwidth of the channel between the computer's memory and CPU), the power wall (the chip's overall temperature handling capacity and power consumption), and the instruction level parallelism (ILP) wall (the availability of enough discrete parallel instructions for a multi-core chip). The latter bottleneck is mostly dependent on the computer's instruction set architecture (ISA) and the availability of the resources and is beyond the scope of this work. However, the earlier two bottlenecks are dependent on the low-level design issues (circuits, interconnect). If we closely observe the clock frequency trend of the microprocessor over the last twenty-four years, we can easily predict that the upcoming years the processor speed will settle down in the frequency range of 3–5GHz, as shown in Figure 1 [1]. This bandwidth limitation is largely because of overall power consumption of the system and the available cooling systems. The situation is even more critical for portable mobile devices, such as laptops, tablets, and phones, where the power wall hits much earlier. This is primarily due to the constraints of battery capacity and limited or often fanless cooling.

Due to the advancement of CMOS technology, the density of transistors and the speed of integrated circuits have gone through a tremendous revolution in

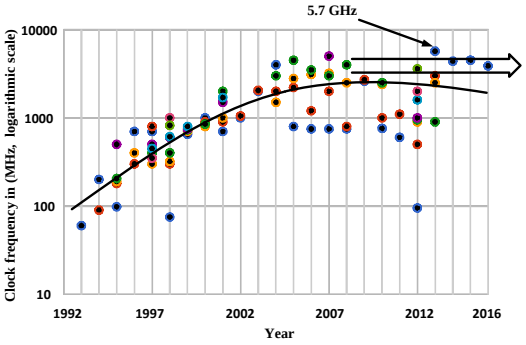

Figure 1: Due to the bottleneck of the power wall, battery capacity, and existing cooling systems, the modern microprocessor clock frequency has settled down in the range of 3–5GHz [1].

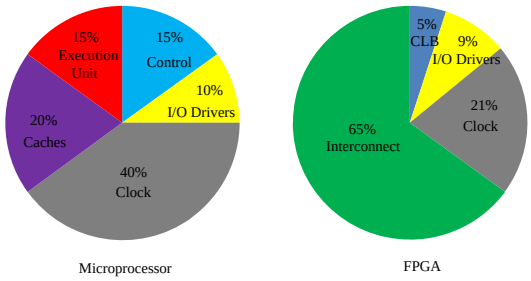

Figure 2: Interconnect and clocks constitute the majority of the dynamic power budget for microprocessor and FPGA [4].

the last five decades [2]. The silicon industry follows Moore's law where the number of transistors integrated in a single die grows exponentially [3]. The huge number of transistors in a die has led the silicon industry to integrate all the digital, analog, and data communication modules in a single chip. However, most system-on-chips (SOCs) are interconnect limited, since the interconnect does not scale as well as the transistors. Hence, designing an interconnect within an optimal power and performance budget has become very critical for modern microprocessors.

Due to the increasing number of devices and die size, the International Technology Roadmap for Semiconductors (ITRS) projected the requirement of 12–16 levels of metal interconnect. However, the number of metal layers has not grown much past 10–12. This is mostly due to the overhead of vias in lower metal layers. As a result, the interconnect (i.e., system clock, long buses etc.) delay often exceeds the gate delay. On the other hand, the total interconnect power can vary depending on the application of a system. Figure 2 shows the different power breakdowns of microprocessor and an field-programmable gate array (FPGA) designs [4]. Clearly, from Figure 2, the interconnect and clocks constitute the majority of the power budget for each class of devices.

In this paper, we present an analysis of different voltage- and current-mode signaling schemes. We compare the different signaling schemes in terms of on-chip power, performance, and robustness. In addition, we propose a modified CM signaling scheme using a simple current-comparator-based receiver circuit. In particular, the key contributions of this paper are:

- A head-to-head comparison of several different previous signaling schemes.
- A frequency scaling analysis of the previous schemes considering power and performance.
- The demonstration of a new CM signaling scheme using a simple transmitter and receiver circuit.
- Process-voltage-temperature (PVT) variation analysis of different signaling schemes.

The rest of the paper is organized as follows: Section 2. gives a brief overview of the previous signaling schemes. Section 3. proposes our new CM signaling circuit. Section 4. compares different signaling schemes. Finally, Section 5. concludes the paper.

2. Overview of Existing Signaling Schemes

The advancement of CMOS technology with innovative circuit topologies has increased the speed of synchronous ASICs and SOCs. This creates a demand for high global clock frequency. In general, CMOS signaling schemes are VM, since CMOS signals are terminated in a MOSFET gate, resulting in nearly

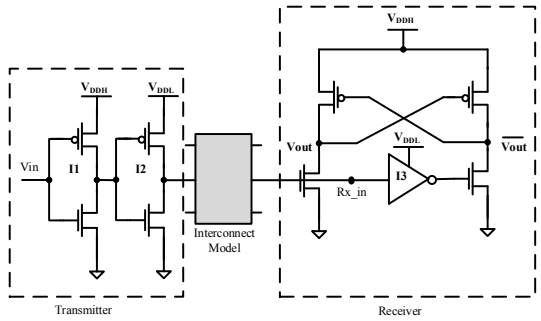

Figure 3: Conventional low-swing schemes utilize dual-supply voltage and a low-swing interconnect to save power [5].

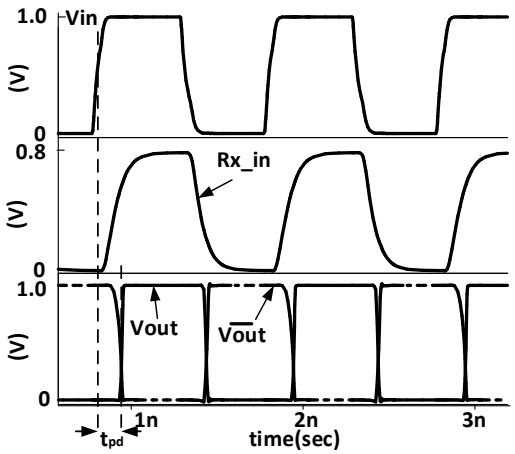

Figure 4: HSPICE simulation confirms the transmission of the low-swing signal over the interconnect and the recovery of full-swing output voltage using the DVSL-based Rx circuit [5].

infinite impedance at the final node. On the other hand, in a CM signaling scheme, we utilize current instead of a voltage signal. The CM signals usually terminate at the final node with a low impedance, making them less sensitive to electrostatic discharge (ESD) stress compared to VM signals.

2.1 Low-Swing Signaling

Reduced or low-swing signaling is very attractive in low-power design, because this method directly improves the energy/bit of an interconnect or data transmission system. A signaling scheme is considered to be efficient according to its dynamic switching energy, design complexity or area/routing, delay, and reliability (i.e., robustness to process variation, voltage supply noise, and crosstalk noise).

A low-swing signaling scheme consists of a transmitter/driver (Tx) and a receiver (Rx) circuit and an interconnect between them. Generally, low-swing schemes are based on level-converter circuits. A conventional low-swing signaling scheme and the simulation results of driving a $5mm$ interconnect are shown in Figure 3 [5] and Figure 4, respectively. This scheme is based on a differential cascode voltage switch Logic (DCVSL)-based Rx circuit. The Tx generates a slow and energy-efficient signal. A DCVSL-type Rx circuit generates a full-swing output signal. This scheme enables large power savings compared to traditional full-swing signaling schemes. However, it is highly susceptible to crosstalk noise.

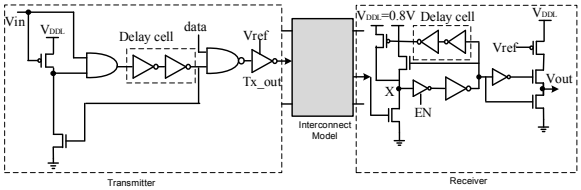

Figure 5: The SRLR-based scheme uses a conventional pulse generation scheme to transmit a low-swing pulsed signal over the interconnect [8].

The pseudodifferential interconnect is another low-swing on-chip interconnect [6]. The Tx or the interconnect driver uses NMOS transistors for both pull-up and pull-down. The Rx circuit is a clocked sense amplifier followed by a static Set-Reset (SR) latch. This scheme has high energy efficiency. However, a mismatch between the two reference signals can cause functional failure or use more energy.

Other researchers presented a self-resetting logic repeater (SRLR)-based low-swing signaling scheme for mesh network-on-chips (NoCs) [8]. Figure 5 and Figure 6 show the SRLR-based signaling scheme and the HSPICE simulation results, respectively. This scheme offers low power; however, it increases the latency due to the low-swing operation and repeaters.

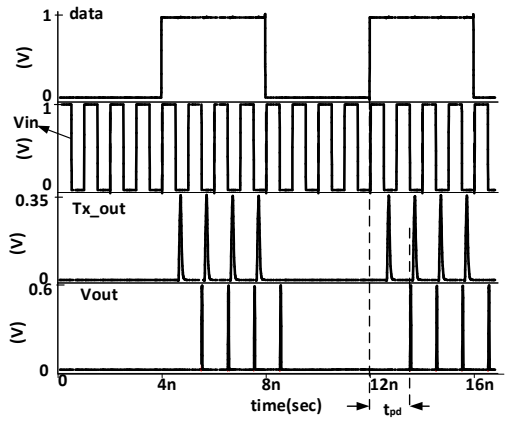

Figure 6: HSPICE simulation confirms the transmission of the low-swing pulse modulated signal over the interconnect and the regeneration of the pulsed signal using the SRLR-based Rx circuit.

2.2 Resonant Energy Recovery Signaling

Resonant signaling uses the clock capacitance and an on-chip inductor to resonate at a fundamental frequency [9]. In order to understand how energy recovery works and saves energy, we explore the dynamic energy dissipation of a traditional CMOS logic gate. Figure 7 shows the output voltage (V_{out}) and charging-discharging currents ($i_{V_{DD}}$ - i_{GND}) of a standard CMOS gate. We can calculate the value of the energy E_S, stored on the capacitor at the end of the transition, by integrating instantaneous power over the period using

$$E_s = \int_0^\infty \mathrm{i_{V_{DD}}(t)} V_{out}\, \mathrm{d}t = \frac{C_L V_{DD}^2}{2}, \qquad (1)$$

where V_{DD} is supply voltage. However, we know that the dynamic energy dissipation of each cycle is $C_L V_{DD}^2$. Clearly, from Equation 1, half of the energy (i.e., $\frac{C_L V_{DD}^2}{2}$) dissipates in the process of charging load capacitance at the pull-up network (M_P of Figure 7), while the other half of the energy dissipates in the pull-down network (M_N of Figure 7). Hence, energy recovery signaling recycles the latter half of the energy that dissipates in the pull-down network

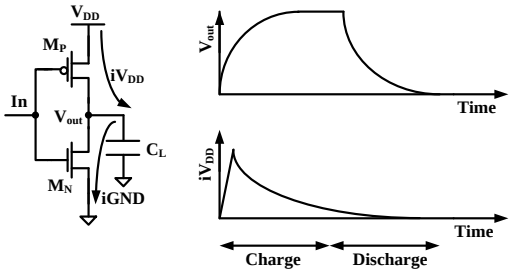

Figure 7: The CMOS gate consumes dynamic power in the process of charging and discharging the output capacitance (C_L).

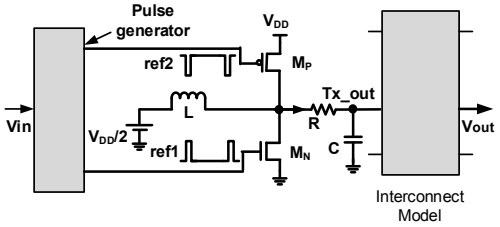

Figure 8: In a resonant signaling scheme, a lumped inductor stores and recycles the returned energy from the circuit capacitance (C) into magnetic energy and periodically charges and discharges through LC resonance to save power [10].

using a lumped inductor.

A traditional resonant circuit that is capable of absorbing the energy stored in the electric field of circuit capacitance is shown in Figure 8. A lumped inductor is employed to store and recycle the returned energy from the circuit capacitance into magnetic energy. Hence, C periodically charges and discharges through LC resonance, resulting in a resonant sinusoidal output at the Tx_{out} node, as shown in Figure 9. The resonant circuit effectively creates a series (RLC) network, and we can write the energy dissipation (E_r) of a resonant circuit as

$$E_r = \frac{\pi}{4Q} C V_{DD}^2 \qquad (2)$$

where Q is the quality factor. Comparing the energy dissipation of a CMOS network (Equation 1) and a resonant energy recovery network (Equation 2) with

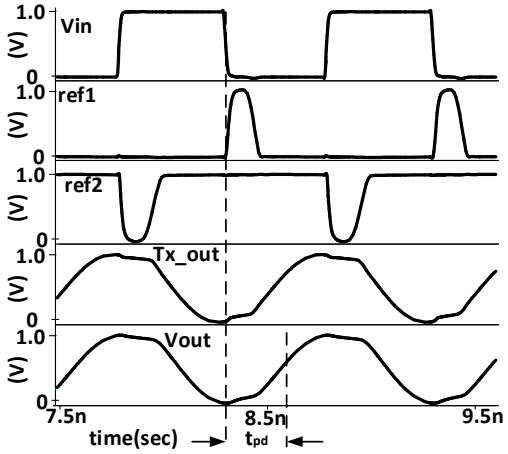

Figure 9: In a resonant signaling scheme, narrow positive and negative pulses are applied to sustain oscillation and to avoid overshoot, respectively.

the same capacitive load, we can come to a break-even point of the quality factor of an (RLC) network at $(Q_{min} > \frac{\pi}{2})$.

All the energy-recovery resonant signaling schemes are frequency limited. In recent years, the narrow frequency range of conventional resonant signaling was eliminated by the application of intermittent resonant signaling (IRS) [11, 12]. However, resonant signaling still requires an extra inductor and inherently has a long signal rise/fall time due to the sinusoidal output signal. We will provide more evidence on that in Section 4..

2.3 Current-Mode Signaling

A CM signaling scheme offers low-energy with higher reliability. Moreover, this scheme is less susceptible to high-energy-particle-induced single-event transients. Nearly 20% of the overall sequential soft error rate is reported due to a clock node upset [13, 14].

In a CM signaling scheme, a Tx utilizes a VM input signal to transmit a current with minimal voltage swing into an interconnect (transmission line), while a Rx converts current to voltage, providing a full-swing output voltage. In the early stages, a CM signaling scheme was applied to current sense

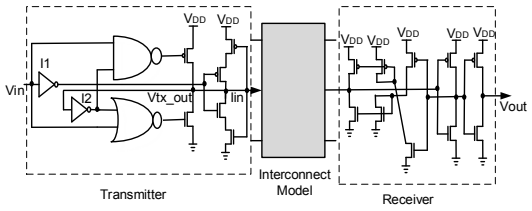

Figure 10: Dynamic over-driving transmitter-based CM scheme uses feedback connection at the receiver circuit to tackle V_{CM} shift, but voltage variation at the long interconnect source and sink nodes can result in rise-time and fall-time mismatch in the output [15].

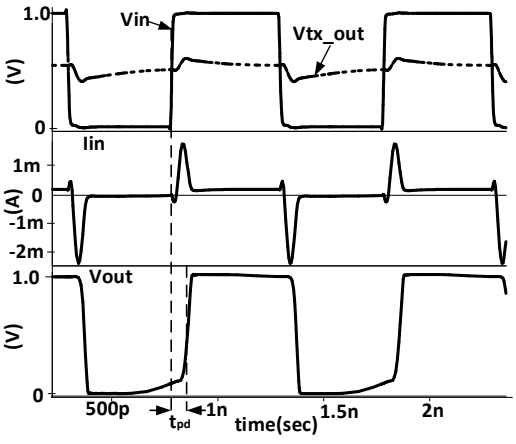

Figure 11: HSPICE simulation confirms the dynamic over driving transmitter-based CM schemes' [15] voltage-to-current and current-to-voltage conversion using the Tx and the Rx circuits, respectively.

amplifiers for CMOS static random-access memories (SRAM) [16]. This paper modeled a long interconnects bit line as an RC network and analytically showed the significant improvement of CM signaling delay compared to VM signaling.

Another interesting CM signaling scheme was reported by Katoch and his colleagues [15], as depicted in Figure 10. The scheme is based on a dynamic over-driving Tx with a strong and weak driver.

The Rx circuit consists of a low-gain inverter amplifier and a controlled current source. The feedback from the amplifier provides the necessary bias voltage

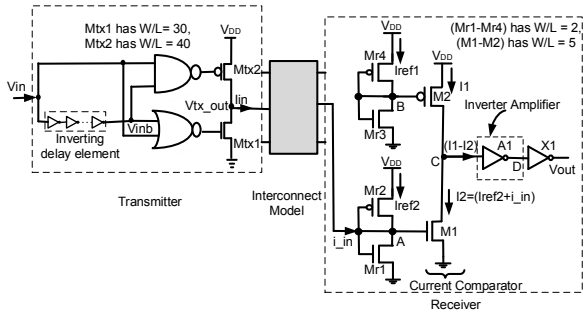

Figure 12: The proposed CM signaling scheme uses a simple NAND-NOR gate-based transmitter to drive and distribute a push-pull current into the interconnect; the receiver circuit is based on a current comparator and effectively accepts a push-pull current and converts into a full-swing output voltage.

at the input node of the Rx network for appropriate current sensing. Moreover, this scheme tackles the problem associated with the Rx line common-mode voltage (V_{CM}) swing by using feedback at the Rx circuit. HSPICE simulation confirms the voltage-to-current and current-to-voltage conversion using the dynamic over driving Tx and the Rx circuits, respectively, driving a $5mm$ interconnect. However, due to the long transmission line it is likely to have different voltages at the Tx output and the Rx input nodes, resulting in slew-rate mismatch in the output.

3. Proposed Current-Mode Signaling

All of the previous CM signaling schemes utilized a complex current-to-voltage converter as a current Tx circuit and/or a complex voltage-to-current converter as a current Rx circuit. Although, our proposed CM signaling scheme adopts similar concept, the architectures of the proposed Tx and Rx circuits are much simpler than those of the previous schemes. Our CM scheme is based on a current-comparator (CC)-based Rx circuit, as shown in Figure 12.

The operation of the proposed CM signaling scheme can be explained using Figure 12 and Figure 14. The proposed Rx circuit has reference-voltage generators, a CC stage, an inverter-amplifier, and an

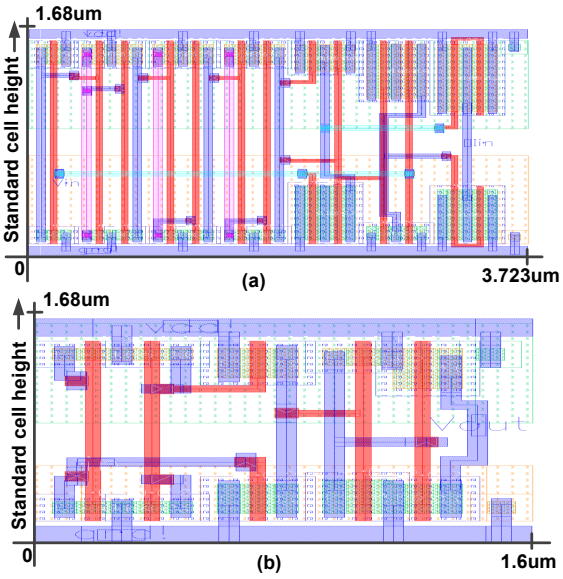

Figure 13: We used standard cell height to design (a) the CM Tx and (b) the proposed CM Rx circuit.

output driver inverter, as shown in Figure 12. The reference-voltage generator, Mr3–Mr4 creates a reference current (Iref1) that is mirrored by M2 to generate I1. The reference-voltage generator Mr1–Mr2 generates reference currents Iref2. The Rx circuit combines Iref2 with the input-current (i_in), and the combined current is then mirrored by M1 to I2. An inverter amplifier (A1) compares two mirrored currents at its input node C and is extended to a CMOS logic level at node Vout by an output inverter (X1). The correct functionality of the proposed scheme depends on the sizing of the reference-voltage generators and the CC. For the reference-voltage generators (Mr1–Mr4) and the CC (M1–M2), we used transistor aspect ratios ($\frac{W}{L}$) of 2 and 5, respectively. Figure 13(a) and Figure 13(b) show the proposed CM signaling Tx and the Rx circuit layouts, respectively.

The current Rx circuit is sensitive to a push-pull input current and enables a simple Tx circuit. In addition, the Tx circuit should provide a stable output voltage that sets the bias point of the Rx circuit. For this we used a simple NAND-NOR based Tx circuit [17], as shown in Figure 12. Similar to previous signaling schemes, the Tx circuit accepts a full-swing

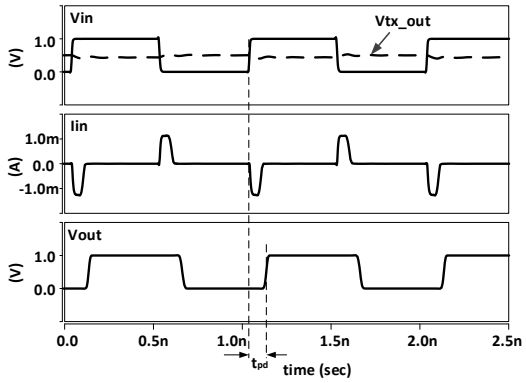

Figure 14: HSPICE simulation results of the proposed scheme confirm that a voltage-mode input is converted to a constant interconnect voltage and a representative push-pull current at the receiver circuit.

input voltage (Vin) and converts it into a push-pull current. The NAND-NOR gates use the Vin and a delayed version of Vin to generate a small negative and a small positive pulse at the rising and falling edges of Vin signal. The NAND gate uses the Vin signal and a delayed inverted version of the Vin signal (Vinb), using the inverted delay element as input to generate a negative pulse. The negative pulse briefly turns ON the PMOS Mtx2 to deliver a push-current on the interconnect. On the other hand, the NOR gate generates a small positive pulse on the falling edge of the Vin signal to briefly turn ON the NMOS transistor Mtx1 that pulls current from the interconnect. The sizing of Mtx1 and Mtx2 is critical to set up the bias voltage and transmit enough current for the Rx circuit. In order to drive a $5mm$ interconnect wire, we used Mtx1 and Mtx2 transistors with $\frac{W}{L}$ of 30 and 40, respectively.

Figure 14 shows the HSPICE simulation results of the proposed CM signaling scheme. The Tx converts the VM input into a push-pull current (Iin) and a near-constant voltage (Vtx_out). The Rx circuit converts the input current (i_in) into a full-swing output voltage (Vout) using a CC, an inverter amplifier, and an output inverter.

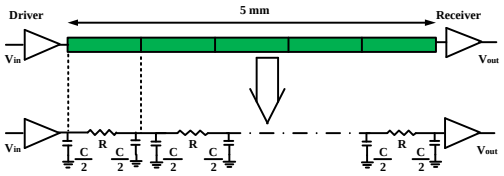

Figure 15: In order to measure the power-performance of different signaling schemes, we used a $5mm$ interconnect line modeled as a distributed RC network driven by respective Tx circuits, and the final node of the interconnect is connected to the Rx circuits to provide a full-swing output voltage.

4. Experiments

4.1 Experimental Setup

In order to compare the propagation delay (t_{pd}), power consumption, and average rise/fall time (t_{rf}) of different schemes, we implemented a test network using a $5mm$ interconnect wire as shown Figure 15. The interconnect RC parasitics were extracted from a predictive technology model (PTM) [18] considering a top global metal layer using a CMOS 45nm technology interconnect $width = 0.8\mu m$, $spacing = 0.8\mu m$, $thickness = 2\mu m$, $height = 1\mu m$, $dielectric\ constant = 2.5$.

In this experiment, we implemented the conventional level converter circuit-based low-swing scheme [5], an SRLR-based low-swing signaling scheme [8], a resonant energy recovery signaling [19], a dynamic over driving Tx-based traditional CM (TraCM) signaling scheme [15], a traditional buffered VM scheme, and our proposed CM signaling scheme. Each circuit uses a 45nm CMOS technology [20]. The power performance of each scheme was evaluated considering frequencies of 1–$3GHz$ (typical clock frequency ranges) and a 1V supply voltage. However, for the low-swing scheme, in addition to a regular supply voltage, we used a low supply voltage ($V_{DDL} = 0.8V$ for [5] and $V_{DDL} = 0.4V$ for [8]).

4.2 Power-Performance Comparisons

Table 1 shows the propagation delay (t_{pd}), power (P, static and dynamic), average rise-fall time (t_{rf}), and

Table 1: In the 1–3GHz frequency range, the buffered VM signaling scheme consumes the highest power, and the proposed CC-based CM signaling scheme consumes the lowest power.

Signaling schemes	Frequency											
	$1GHz$				$2GHz$				$3GHz$			
	$t_{pd}(ps)$	$t_{rf}(ps)$	$P\ (mW)$	$PDP\ (fJ)$	$t_{pd}(ps)$	$t_{rf}(ps)$	$P\ (mW)$	$PDP\ (fJ)$	$t_{pd}(ps)$	$t_{rf}(ps)$	$P\ (mW)$	$PDP\ (fJ)$
Buffered	156.2	23.2	1.91	298.3	156.6	23.3	3.83	599.8	155.8	22.7	5.73	892.7
Low-swing [5]	146.3	16.3	1.0	146.3	144.0	16.4	1.99	286.6	143.0	15.4	2.68	383.2
Resonant [9]	212.6	110.2	0.85	210.5	210.3	100.2	1.0	361.7	208	100.0	1.9	545.0
TraCM [15]	73.6	70.5	0.8	58.9	68	30.3	1.14	77.5	57.1	129.8	1.58	136.5
SRLR [8]	1469.0	28.0	0.37	562.4	1490.0	25.0	0.43	642.2	1355.0	23.0	0.72	971.5
Our CM	98.0	24.0	0.15	15.0	93	20.0	0.26	24.2	97.0	21.0	0.37	35.9

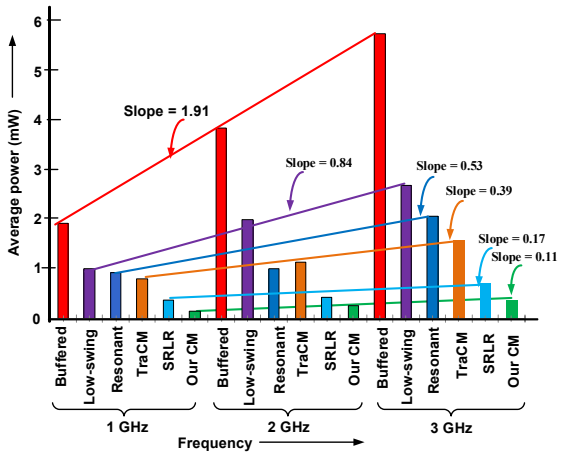

Figure 16: The proposed CM scheme consumes 92% to 95% less power compared to the traditional buffered VM signaling scheme at 1–3GHz frequency and the dynamic power increase proportional to frequency in the CM scheme ($slope = 0.11$) is at a much slower rate than in the VM scheme ($slope = 1.91$).

power-delay product (PDP) comparison of the different signaling schemes. As expected, the buffered VM signaling scheme consumes the highest power at all the frequencies due to the full voltage swing on the interconnect. On the other hand, among other analyzed existing signaling schemes, the dynamic over-driving Tx based CM scheme consumes the lowest power due to the negligible voltage swing on the interconnect. In particular, the TraCM scheme [15] consumes 58% to 72% less power compared to the buffered VM signaling scheme at 1–3GHz frequency, as shown in Figure 16. The proposed CM scheme consumes 92%, 93%, and 95% less power compared to the buffered signaling scheme at $1GHz$, $2GHz$, and $3GHz$, respectively. In addition, the proposed scheme consumes 77% to 81% less average power compared to the TraCM [15] scheme. At $3GHz$ frequency, the proposed scheme consumes 48% lower power compared to the recently reported SRLR scheme [8].

Among all the signaling schemes, TraCM signaling has the lowest t_{pd} and the SRLR-based low-swing signaling scheme has the largest t_{pd}. At $3GHz$, the resonant scheme has 58.5% higher t_{pd} than the TraCM [15] signaling scheme due to the large Tx delay. In addition, resonant signaling consumes 1.7× more power and has 4.8× higher slew than the TraCM scheme. At $3GHz$ frequency, the proposed CM has 11% extra latency and equal slew rate compared to the TraCM [15] scheme. However, the proposed CM scheme has 73.7% lower PDP than the TraCM scheme.

In order to understand the scaling of the different signaling schemes, we considered different wire lengths, ranging from $1mm$ to $5mm$. The power consumption of the different signaling schemes at $1GHz$ frequency is shown in Figure 17. As expected, all the signaling power consumption increases primarily linearly with the increase of wire length. However, the rate of increase of power consumption of the proposed scheme proportional to the length is much lower than that of the buffered scheme.

4.3 Process-Voltage-Temperature (PVT) Variation Analysis

The performance of a signaling scheme is significantly affected by transistor threshold voltage (V_{th}) varia-

Table 2: The proposed signaling scheme exhibits similar or better robustness to process-voltage-temperature variation compared to other state-of-the-art schemes.

Signaling schemes	V_{th}–variation			V_{DD}–variation			Temperature–variation		
	$t_{pd}^{ff}(ps)$	$t_{pd}^{ss}(ps)$	% range	$t_{pd}^{1.1}(ps)$	$t_{pd}^{0.9}(ps)$	% range	$t_{pd}^{-25°C}(ps)$	$t_{pd}^{125°C}(ps)$	% range
Buffered	125.9	314.0	−19.4 to 50.3	145.2	173.6	−10.0 to 7.0	125.4	248.6	−19.7 to 37.2
Low-swing [5]	107.9	397.6	−26.2 to 63.2	141.4	146.3	−3.8 to 3.5	116.1	228.1	−20.6 to 35.9
Resonant [9]	177.1	349.3	−16.7 to 39.1	201.2	236.0	−9.9 to 5.4	185.5	301.2	−12.5 to 29.4
TraCM [15]	53.0	243.4	−28.0 to 69.8	62.4	91.7	−19.7 to 15.2	57.1	129.8	−22.4 to 43.3
SRLR [8]	1013.0	1860.0	−31.0 to 21.0	1265.0	1650.0	−11.0 to 13.9	1121.5	2432.0	−23.7 to 39.6
Our CM	83.0	221.0	−15.3 to 55.7	91.5	102.2	−4.1 to 6.6	78.0	156.6	−20.4 to 37.4

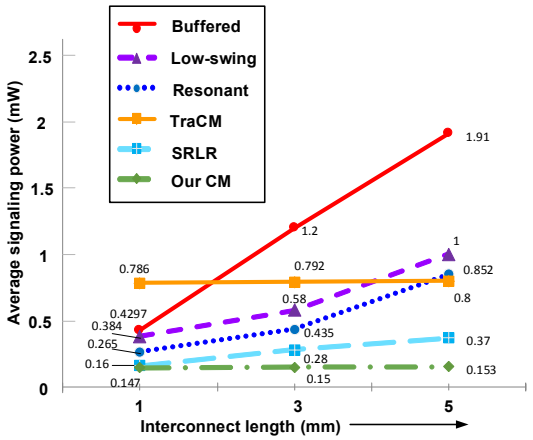

Figure 17: The signaling power increases linearly with the increase of interconnect length; however, the rate of increase of power consumption of the proposed scheme proportional to the length is much lower than the buffered scheme.

tion. The primary sources of this variation are the doping concentration, gate oxide thickness, effective gate length, etc. [21]. In this analysis, we considered worst-case corners fast-fast (ff) and slow-slow (ss) transistors. The TraCM and SRLR schemes have −28% to 69.8% and −31% to 21% t_{pd} variation, respectively, due to V_{th}-variation. The proposed CM signaling scheme has −15.3% to 55.7% t_{pd}-variation due to V_{th}-variation, as shown in Table 2.

Due to IR-loss, the V_{DD} can vary and is considered one of the major sources of circuit performance variation. For this analysis, we considered ±10% V_{DD} variation. The proposed scheme shows −4.1% to 6.6% t_{pd} variation compared to the larger −10.0% to 7.0% t_{pd} variation using the standard buffered VM scheme. The primary reason for this improvement is the absence of buffers in the interconnect.

In nanoscale technology, temperature variation can significantly affect the performance of a signaling scheme. In order to analyze the temperature-variation-induced t_{pd}, we considered $-25°C$ to $125°C$ temperature variation from the nominal temperature ($25°C$). The extracted HSPICE simulation results are shown in Table 2. According to our analysis, the proposed CM scheme has 5.5% lower delay variation compared to the SRLR-based scheme.

5. Conclusion

In this paper, we presented different existing low-power VM and CM signaling schemes. We also proposed a CC-based low-power CM signaling scheme. In order to compare efficiency, we performed analysis by implementing the different signaling schemes on a $5mm$ interconnect line. Among other analyzed existing schemes, the dynamic over driving Tx-based TraCM [15] scheme consumes the lowest power, while the traditional buffer-based VM scheme consumes the highest power. However, the proposed CM scheme consumes up to 94% and 81% lower power compared to the buffered VM and TraCM [15] schemes, respectively. In addition, the proposed CM signaling has 37% to 41% lower latency and equal slew-rate compared to the buffered signaling scheme. However, the most important observation of these experiments was that the power consumption of the CM scheme increases proportionally to frequency at a much slower rate than the other signaling schemes, as shown in

Figure 16.

ACKNOWLEDGMENT

The author would like to thank Professor Matthew Guthaus from UCSC for scientific discussion, software support, and inputs.

REFERENCES

[1] ISSCC 2013 Supplement, Available: http://isscc.org/index.html.

[2] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Prospective*. Second Edition, Prentice Hall, 2003.

[3] Gordon E. Moore, "Cramming more components onto integrated circuits," *IEEE Solid-State Circuits Society Newsletter*, Vol. 38, no. 8, pp. 114, April 1965.

[4] J. Rabaey, *Low Power Design Essentials*. Second Edition, Springer Science and Business Media, 2009.

[5] Y. Nakagome, B. K. Itoh, M. Isoda, K. Takeuchi, and M. Aoki, "Sub-1-V swing internal bus architecture for future low-power ULSIs," *IEEE Journal of Solid-State Circuits*, Vol. 28, no. 4, pp. 414–419, April 1993.

[6] H. Zhang, and J. M. Rabaey, "Low-swing interconnect interface circuits," *IEEE International Symposium on Low Power Electronics and Design*, New York,1998, pp. 161–166.

[7] H. Zhang, V. George, and J. M. Rabaey, "Low swing on-chip signaling techniques: effectiveness and robustness," *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 8, no. 3, pp. 264–272, June 2000.

[8] S. Park, M. Qazi, L. S. Peh, and A. P. Chandrakasan, "40.4fJ/bit/mm low-swing on-chip signaling with self-resetting logic repeaters embedded within a mesh NoC in 45nm SOI CMOS," *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2013, pp. 1637–1642.

[9] R. Islam, "Low-Power Resonant Clocking Using Soft Error Robust Energy Recovery Flip-Flops," *Journal of Electronic Testing*, Vol. 34, no. 4, pp. 471–485, August 2018.

[10] V.S. Sathe, S. Arekapudi, A. Ishii, C. Ouyang, M.C. Papaefthymiou, and S. Naffziger, "Resonant-Clock Design for a Power-Efficient, High-Volume x86-64 Microprocessor," *IEEE Journal of Solid-State Circuits*, Vol. 48, no. 1, pp. 140–149, January 2013.

[11] H. Fuketa, M. Nomura, M. Takamiya, and T. Sakurai, "Intermittent Resonant Clocking Enabling Power Reduction at Any Clock Frequency for Near/Sub-Threshold Logic Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 49, no. 2, pp. 536–544, January 2014.

[12] I. Bezzam, S. Krishnan, T. Raja, and C. Mathiazhagan, "An Energy-Recovering Reconfigurable Series Resonant Clocking Scheme for Wide Frequency Operation," *IEEE Transactions on Circuits and Systems I*, Vol. 62, no. 7, pp. 1766–1775, July 2015.

[13] G. C. Messenger, "Collection of charge on junction nodes from ion tracks," *IEEE Transaction on Nuclear Science*, Vol. 29, no. 6, pp. 2024–2031, December 1982.

[14] R. Islam, "High-speed Energy-efficient Soft Error Tolerant Flip-flops," *M.A.Sc. Thesis*, Concordia University, Montreal, Canada, 2011.

[15] A. Katoch, H. Veendrick, and E. Seevinck, "High Speed Current-mode Signaling Circuits for On-Chip Interconnects," *IEEE International Symposium on Circuits and Systems*, Kobe, Japan, 2005, pp. 4138–4141.

[16] E. Seevinck, P. J. V. Beers, and H. Ontrop, "Current-mode techniques for high-speed VLSI circuits with application to current sense amplifier for CMOS SRAM's," *IEEE Journal of Solid-State Circuits*, Vol. 26, no. 4, pp. 525–536, April 1991.

[17] R. Islam, and M. R. Guthaus, "Low-Power Clock Distribution Using a Current-Pulsed Clocked Flip-Flop," *IEEE Transactions on Circuits and*

Systems I, Vol. 62, no. 4, pp. 1156–1164, April 2015.

[18] Nanoscale Integration and Modeling (NIMO) Group at ASU, "Predictive Technology Model (PTM)," Available: http://ptm.asu.edu/.

[19] W. Athas, N. Tzartzanis, W. Mao, R.Lai, K. Chong, L. Peterson, and M. Bolotski, "Clock-powered CMOS VLSI graphics processor for embedded display controller application," *IEEE International Solid-State Circuits Conference*, 2000, pp. 296–297.

[20] NCSU, FreePDK45, Available: http://www.eda.ncsu.edu/wiki/FreePDK45.

[21] J.P. de Gyvez and R. Rodriguez-Montanes, "Threshold voltage mismatch (ΔVT) fault modeling," *IEEE VLSI Test Symposium*, April 2003, pp. 145–150.

Author's Biography

Riadul Islam is currently an assistant professor in the Department of Electrical and Computer Engineering at the University of Michigan-Dearborn, MI 48128. In his Ph.D. dissertation work at UCSC, Dr. Islam designed the first current-pulsed flip-flop/register that resulted in the first-ever one-to-many current-mode clock distribution networks for high-performance microprocessors. He received his M.A.Sc. degree in Electrical and Computer Engineering from Concordia University, Montreal, Canada, in 2011. From 2007 to 2009, he worked as a full-time faculty member in the Department of Electrical and Electronic Engineering of the University of Asia Pacific, Dhaka, Bangladesh. He is a member of the IEEE, IEEE Circuits and Systems (CAS) society. He holds one US patent and has had several IEEE/ACM journal and conference publications in TVLSI, TCAS, ISCAS, MWSCAS, ISQED, and ASICON. His current research interests include digital, analog, and mixed-signal CMOS ICs/SOCs for a variety of applications; verification and testing techniques for analog, digital and mixed-signal ICs; CAD tools for design and analysis of microprocessors and FPGAs; automobile electronics; and biochips.