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On the advancements of digital signal processing hardware and algorithms enabling the Origins Space Telescope

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Abstract. On August 22, 2019, the Origins Space Telescope (OST) Study Team delivered the OST Mission Concept Study Report and the OST Technology Development Plan to NASA Headquarters. A key component of this study report includes the technology roadmap for detector readout and how new radio frequency-system-on-chip (RFSoC)-based technology would be used to advance the far-infrared polarimeter instrument concept for a spaceflight mission. We present our current results as they pertain to the implementation of algorithms, hardware, and architecture for instrument signal processing of this proposed observatory using RFSoC technology. We also present a small case study, comparing a more conventional readout system with one based on the RFSoC and show a trade of system complexity versus technology readiness level. © *The Authors. Published by SPIE under a Creative Commons Attribution 4.0 Unported License. Distribution or reproduction of this work in whole or in part requires full attribution of the original publication, including its DOI.* [DOI: 10.1117/1.JATIS.7.1.011018]

1 Introduction

The Origins Space Telescope (OST) is one of four large astrophysics mission concepts under consideration for the National Research Council's 2020 Astronomy Astrophysics Decadal Survey[1] (Fig. 1). The far-infrared imager and polarimeter (FIP), one of three baseline science instruments proposed on this observatory, will perform broadband imaging from 50 to 500 μm.[2] To accomplish this, the FIP camera will utilize an image sensor based on arrays of thousands of densely packed microwave frequency-division multiplexed superconducting detectors. The detectors will be composed of transition-edge sensors (TESs) or microwave kinetic inductance detectors (MKIDs). Both MKID and TES arrays are read out similarly, using nearly identical signal processing electronics and methodologies. A key component technology upon which the FIP readout electronics is currently based is a relatively new processor known as the radio frequency system-on-chip (RFSoC), invented by Xilinx.[3] This paper discusses the readout electronics architecture and signal processing flow of the FIP instrument and how the RFSoC plays an important role in its development, from hardware electronics and scientific signal processing perspectives. In addition, this paper presents a trade of technology-readiness-level (TRL) versus power for the FIP readout electronics and presents a TRL-6 path for the flight instrument that can be achieved relatively quickly.

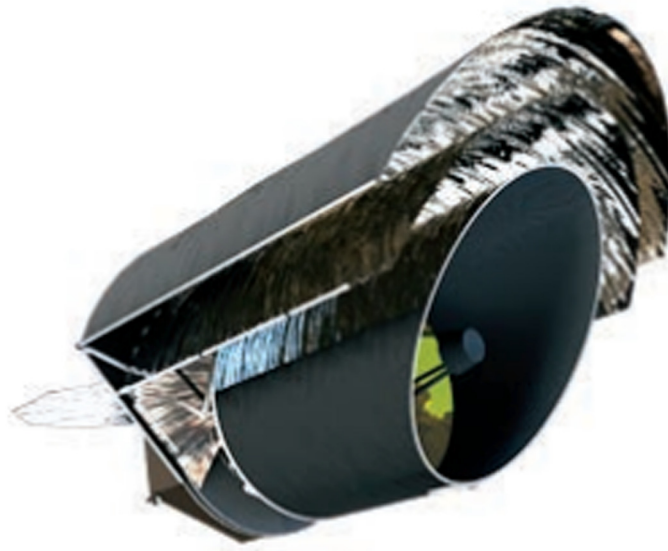*Address all correspondence to Damon C. Bradley, damon.c.bradley@nasa.gov

Fig. 1 Artist conception of the OST.

1.1 *FIP Image Sensor Signal Flow*

The FIP imaging system will feature a new kind of image sensor comprised of arrays of MKIDs or microwave superconducting quantum interference device (SQUID) multiplexed TES resonator elements (pixels). Arrays of the latter type of sensor are the current baseline for the instrument,[1] employing 7957 pixels to be exact. Currently, four groups of ~2000 pixels each are output from the image sensor as RF signals that are amplified by high electron-mobility transistor-based amplifiers. Each signal is 4 GHz in bandwidth and will be located from 4 to 8 GHz in RF frequency. The image sensor also requires detector bias signals, fluxramp modulation signals, and feedback signals to operate. The flow of input and output signals to and from the detector is shown in Fig. 2. The task of the FIP readout electronics subsystem is to acquire and process all four image sensor output signals and generate the feedback, bias, and fluxramp signals required for operation. If MKIDs are used in lieu of TES detectors, then the fluxramp modulation signals are not required.
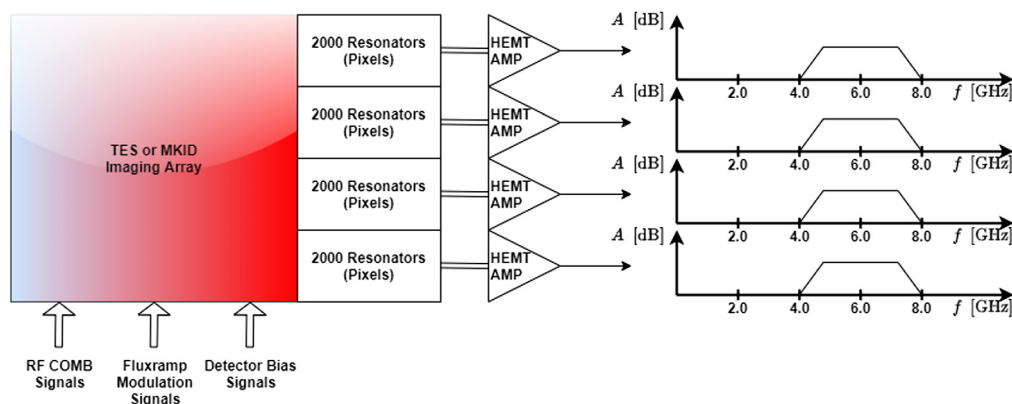

Fig. 2 Detector input and output signals for the FIP instrument. All detector pixels are arranged in four groups of ~2000 each that are passed on to a HEMT amplifier. The signals occupy a 4 GHz bandwidth centered at 6-GHz RF. The detector array also requires a RF comb signal for feedback, as well as fluxramp modulation (only if TES detectors are used) and detector bias signals.
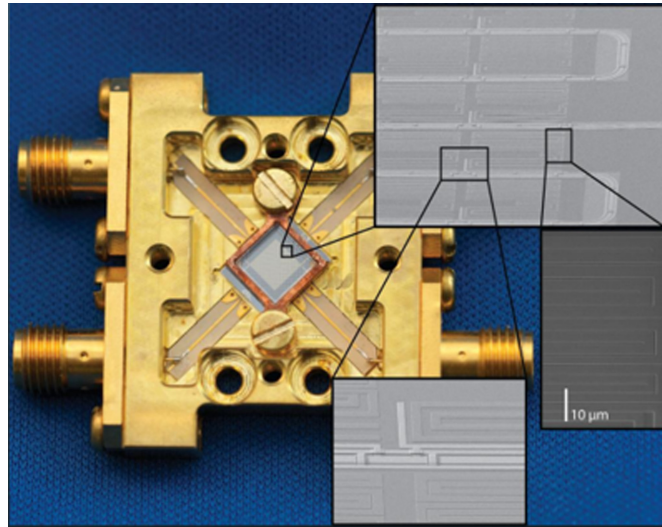
Fig. 3 MKID device, highlighting the lithographically etched resonator arrays along a single feedline.

1.2 *MKID Signal Processing*

MKIDs are a type of cryogenic superconducting photon detector first developed at the California Institute of Technology and NASA Jet Propulsion Laboratory in 2003[4] (Fig. 3). These devices are used for high-sensitivity astronomical detection of electromagnetic frequencies ranging from the far-infrared to x-rays. Impinging photons incident on a strip of superconducting material break Cooper pairs and create excess quasiparticles. The kinetic inductance of the superconducting strip varies inversely with the density of Cooper pairs, and thus the kinetic inductance increases upon photon absorption. This inductance is combined with a capacitor to form a microwave resonator modeled as an equivalent LC tank circuit, with a resonant frequency that varies with the absorption of photons (Fig. 4). An imaging array is formed by connecting many thousands of resonators in parallel along a common transmission line. Since each resonator can be designed to have its own unique starting resonant frequency and corresponding bandwidth, the resonator is said to be frequency-division multiplexed as a result (Fig. 5). Therefore, resonator array readout is accomplished by tracking each resonator frequency response in the transmission line and mapping amplitude, phase, and frequency variation to the amount of kinetic inductance present and, hence, the properties of the incident photon.

The prevailing technique for array readout digitally synthesizes a comb signal, feeds it to the array, and reads back the resulting signal for processing.[5] The comb signal consists of a linear combination of sinusoidal tones that are individually set to the corresponding initial
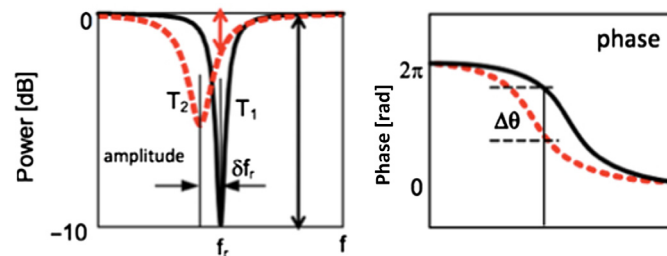

Fig. 4 When an incident photon interacts with the MKID device, the resonator frequency and phase responses are shifted. Measuring this shift is the job of the readout system, and the astrophysical image pixel to be read out is embedded in this shift information.
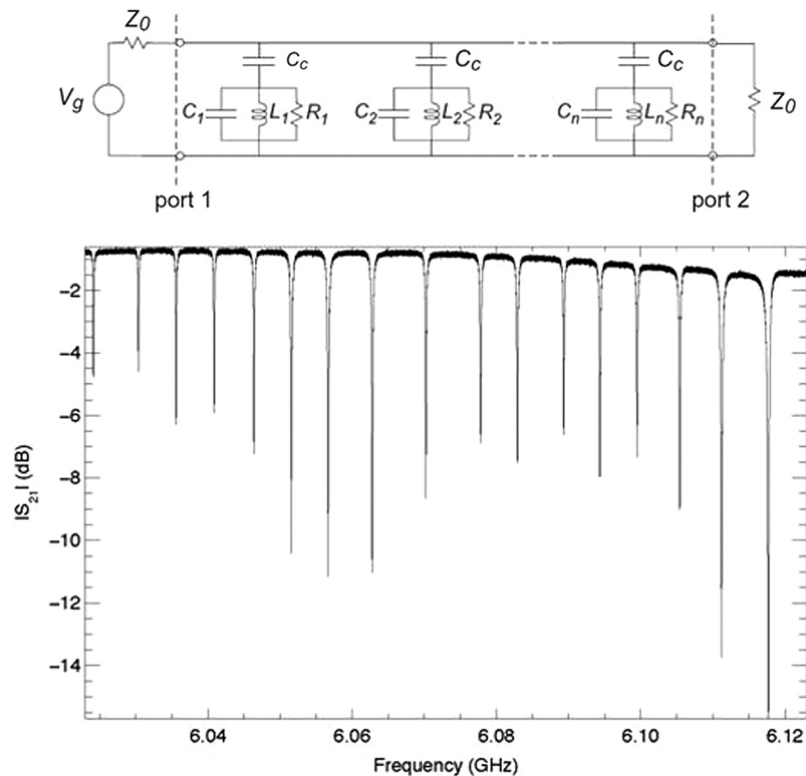
Fig. 5 Equivalent parallel LC circuit representation for a MKID array of *n* resonators and its corresponding frequency response (S_{21} parameter). Figure from Day et al.[4]

frequencies of each detector in the array. As kinetic inductance occurs as a result of incident photons, each sinusoid in the comb signal is modified by its corresponding detector. The resultant output signal is fed back to the electronics system, where its spectrum is estimated, and the modification of each sinusoidal element in the feedback comb signal is computed. Embedded in the output spectra of the instrument is the astrophysical image to be synthesized via ground processing.

1.3 *TES Signal Processing*

A TES, developed in the 1940's by Andrews et al.,[6] is a very sensitive cryogenic energy detector made from a superconducting film held at its phase transition temperature. In this temperature region, a very small change in temperature leads to a very large change in film resistance. An incident photon heats this element, resulting in the resistance change. The superconducting element is inductively coupled to a SQUID resonator array, which is frequency division multiplexed similarly to MKID arrays. Inductively coupling TES devices to a microwave multiplexed SQUID array allows for thousands of TES devices to be utilized simultaneously and share a common RF feedline (Fig. 10).

Readout of TES devices, once multiplexed by microwave SQUID resonators, are read out similarly to MKIDs. The common element between MKID and microwave SQUIDS is the use of a comb signal to excite the microwave resonator array and the use of a spectrometer to measure the resultant spectrum of the comb signal. Compared with MKIDs, TES devices require additional linearization. This is accomplished by means of flux ramp modulation. In this technique, a secondary set of signals are sent to the TES devices so that their responses can be linearized, whereas the primary set of signals are the individual sinusoidal components of the comb signal that address each microwave SQUID resonator element. In this paper, the terminology TES implies frequency-domain SQUID multiplexed variety of TES detectors (Fig. 6).
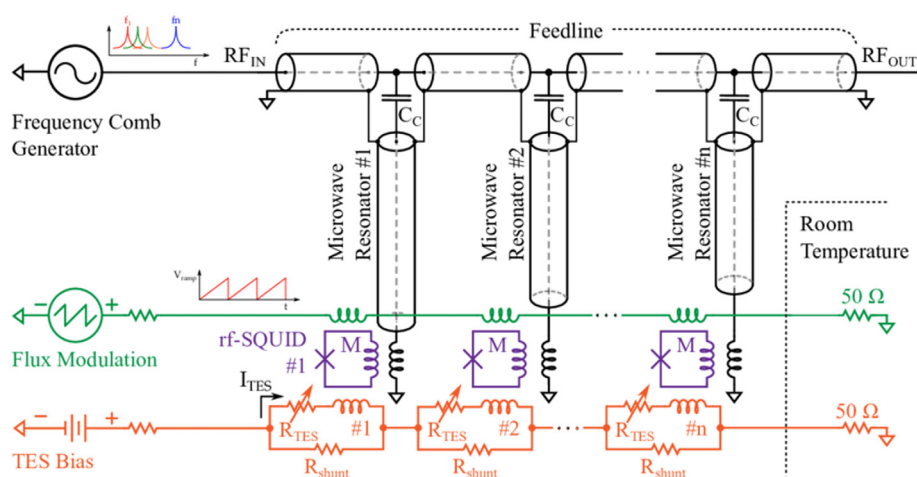
Fig. 6 Microwave-multiplexed TES schematic. Figure from Becker et al.[7]

2 FIP Readout Electronics Hardware

The current design for the FIP readout is based on the Xilinx RFSoC device. This section provides some background on this device, why using it for MKID and TES readout is novel, and the resulting system hardware architecture that supports its use. We show that, for both MKID and TES detector arrays, a single RFSoC device can accomplish all of the digitization and processing for the entire FIP instrument.

3 Digital Signal Processing Using the RF System-on-Chip

The Xilinx RFSoC Generation 1 (Gen-1) is currently a commercial SoC that combines an field-programmable gate array (FPGA), 16 wideband data converters, and one quad-core Arm Cortex-A53 and one dual-core Reduced Instruction Set Computer (RISC-V) processor into a single device[3] (Fig. 7). The data converters consist of eight 4 giga-samples per second (GSPS), 12-bit analog-to-digital converters (ADCs), and eight 6.4 GSPS 14-bit digital-to-analog
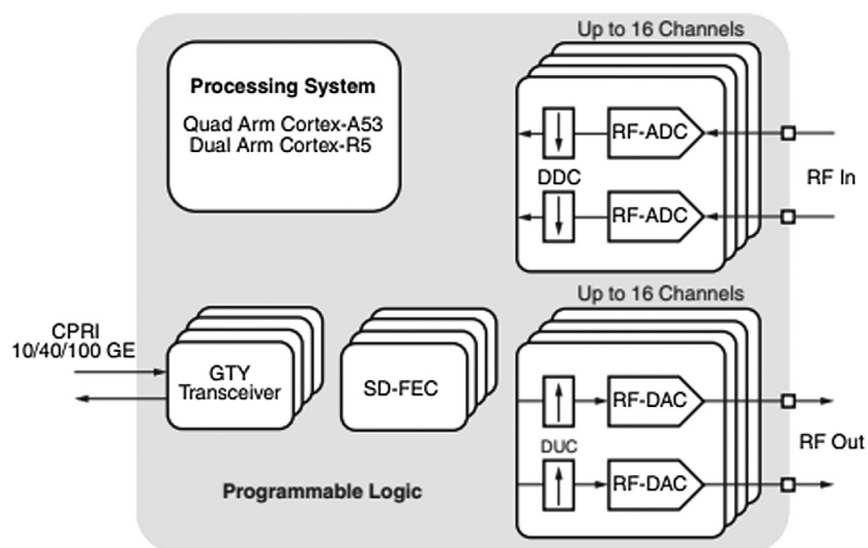

Fig. 7 RFSoC processor from Xilinx. The First Generation (Gen-1) RFSoC, highlighted in this paper, has eight channels of RF input and eight channels of RF output for interfacing to the FIP detector array via a stage of RF downconversion electronics.

converters (DACs). The data converters are independent of each other, can all be synchronized, and are interfaced directly to the FPGA logic in the same chip; therefore, they do not need any any external high-speed data interaces, such as JESD204N, to acquire and process samples. As a result, the FIP input and output RF signals can all be sampled and processed simultaneously by a single RFSoC device, which is commercially available, but not yet space qualified at the time of this writing. Standard FPGA I/O on the same device can also handle control of bias current circuitry and output of digital fluxramp control signals to corresponding low-rate monolithic DACs on the same printed circuit board (PCB) as the RFSoC.

As shown in Fig. 8, development is already underway using an evaluation board provided by Xilinx, which gives access to all of the RFSoC interfaces and FPGA logic for development. A daughter card is necessary to break out the many RF signal I/O and clocking ports.

The novelty of using the RFSoC is that all of the necessary components for digital signal processing are contained within a single chip package, which is unprecedented to date. In particular, we use an RFSoC that has eight ADCs and eight DACs, each operating at more than 12 bits per sample, at sample rates of 4 GSPS, to capture the full bandwidth of the resonator array RF signals. Command and control functions are easily handled in one or more of the many embedded processor cores that come along with the chip. Using an RFSoC as the main processor for the FIP detector readout is functionally optimal since the chip only requires a single PCB to reside on and no other RFSoCs or FPGAs would be necessary.

However, since the RFSoC is not yet radiation hardened, it is necessary to develop a specialized application specific integrated circuit (ASIC) that performs a similar function as the RFSoC that is radiation-hardened. Alternatively, and at the cost of additional power (to be discussed in a later section), conventional spaceflight qualified ADCs, DACs, and FPGAs exist now that can be used in place of the RFSoC. However, using these devices would also require the development of more than one PCB due to the PCB layout for this kind of assembly being significantly complex and multi-layered and requiring precise signal integrity analysis.
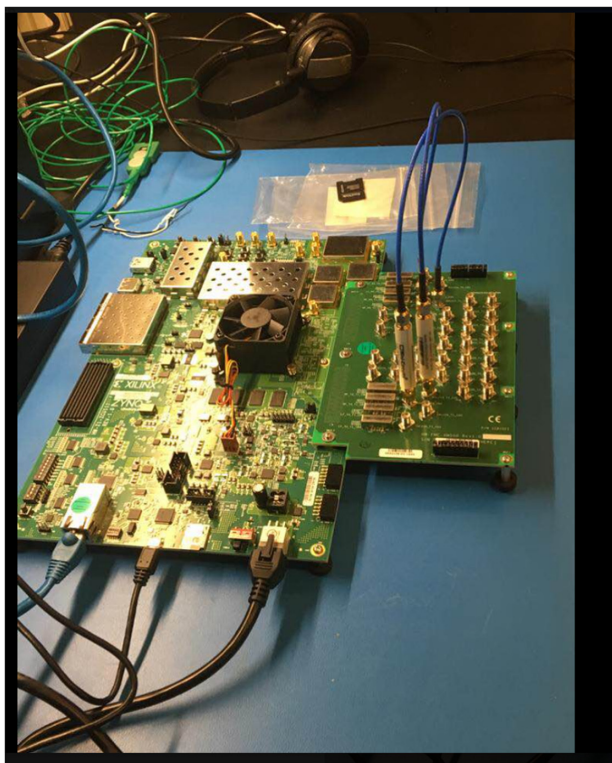

Fig. 8 Xilinx RFSoC development board under test at NASA Goddard Space Flight Center Instrument Electronics Development Branch (Code 564). Courtesy of the Digital Signal Processing Technology Group.

3.1 Frequency Plan

Design of the FIP detector readout electronics system starts with careful consideration of the frequency plan, i.e., the arrangement of the detector signals in the microwave frequency range and the plan for how they arrive at the digital system for subsequent processing. Currently, both TES and MKID detector array designs under consideration for FIP will be designed to operate in the 4 to 8 GHz RF frequency range. This requires all signal processing to synthesize and acquire signals in this range. The Xilinx RFSoC is aptly suited for this task since it has an array of on-chip RF-Sampling ADCs and DACs that sample up to two Nyquist zones and operate at 4 GSPS.

However, the Nyquist bandwidth of each on-chip data converter on the RFSoC under consideration is a maximum of 2 GHz for the ADCs and 3 GHz for the DACs. This means that the entire 4-GHz bandwidth of either the MKID or TES detector array requires 2 DACs and 2 ADCs each for processing. One RFSoC chip therefore is capable of processing 16 GHz of bandwidth; therefore four different groups of 4 GHz detector arrays can be read out simultaneously using only one device. To capture the full 4 GHz of any detector group, while minimizing the amount of required RF analog electronics required for operating in the 4 to 8 GHz band, the bands must be split before interfacing to the RFSoC.

The scheme to accomplish this is shown in Fig. 9. Currently, a group of roughly 2000 microwave resonators (baseline TES or MKIDs) occupy 4 GHz of bandwidth and are presented to the readout system over a single transmission line following a HEMT amplification stage.[1] The full band signal needs to be downconverted and split into two separate 2 GHz-wide bands to be acquired by the on-chip ADCs of the RFSoC. Depending on which Nyquist zone the resulting 2-GHz signal lands—either first or second, a single ADC channel of the RFSoC acquires it since all channels operate at 4 GHz.

FIP outputs four 4 GHz signals, therefore eight ADC channels are required, and the RFSoC has exactly this many ADC inputs to accommodate this. Similarly, the RFSoC has complimentary DACs that can operate at 6 GHz, and they can be used to synthesize the excitation signals that the MKIDs and TES arrays require for readout.

The functional block diagram for the FIP detector readout subsystem is given in Fig. 10. Reading the signal flow from left to right, the TES array (and similarly, the MKID array) produces the RF electrical signals that are captured by all subsequent electronics.

The baseline concept for FIP's image sensor consists of 7957 TES elements, configured as a rectangular array (109×73), and output over four RF transmission lines, with each being 4 GHz
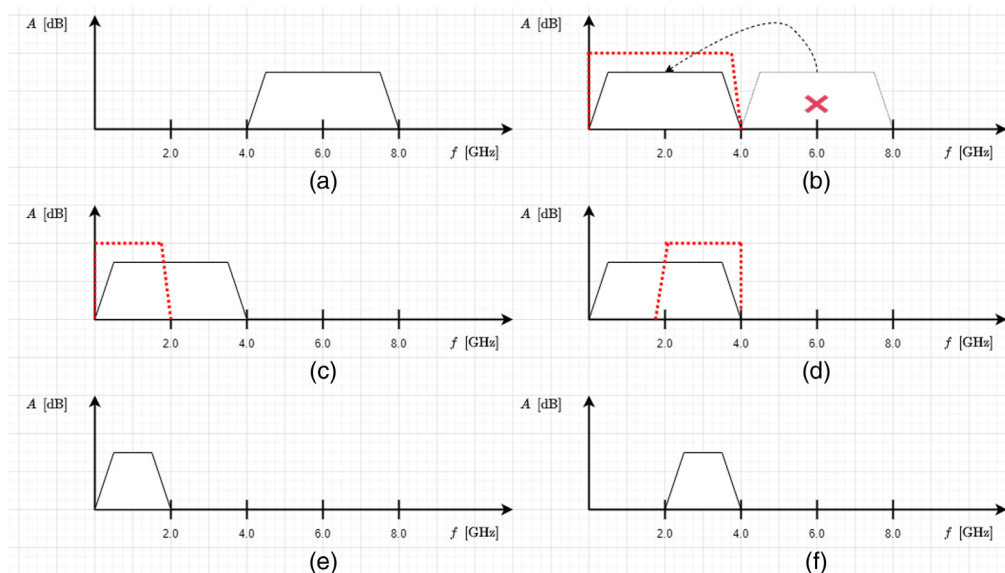

Fig. 9 Detector array frequency plan. The detector resonators live within the 4- to 8-GHz RF bandpass frequency in (a). This signal is downconverted to baseband (0 to 4 GHz), rejecting the image frequency in (b). In (c) through (f), second-Nyquist zone sampling is employed to further downconvert and acquire each signal portion, filtering out image signals along the way.
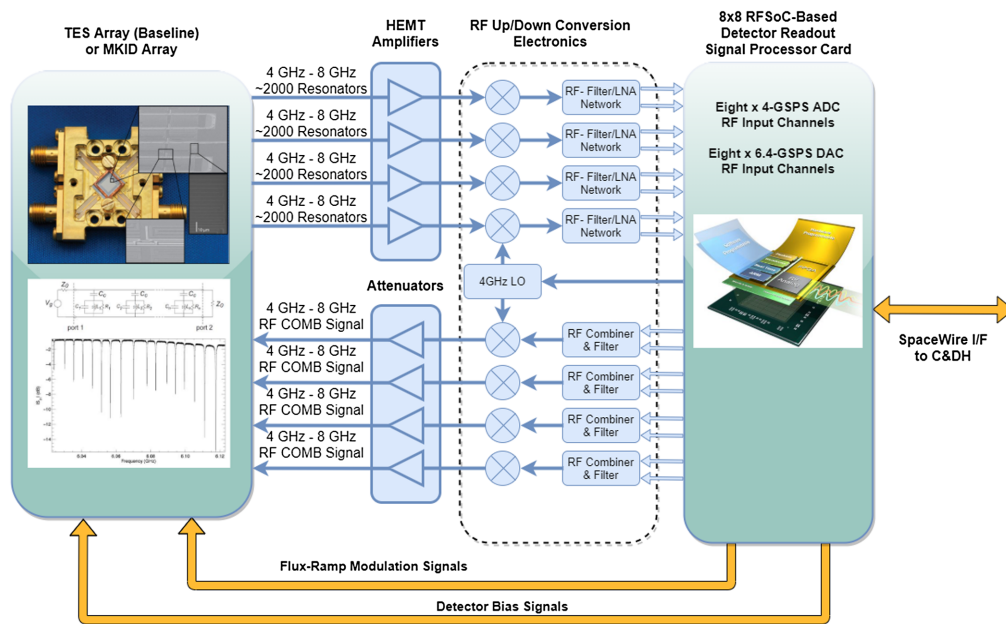
Fig. 10 FIP detector subsystem functional block diagram. Four RF signals corresponding to ~8000 resonators (TES or MKID) interface the input of the system and are processed. Simultaneously, the detector comb signals are synthesized digitally and are fed back via four output RF signals. Two additional sets of outputs consist of flux ramp modulation signals required only for TES detectors for linearizing the array and detector bias currents. Detector array spectra as well as any pertinent system monitoring telemetry are output to the spacecraft computer.

in bandwidth and living in the 4- to 8-GHz RF frequency range. As a result, these four RF signals need to be connected to corresponding HEMT amplifiers and transmitted downstream for readout. The required bandwidth of the FIP detector array is near 16 GHz to cover all TES elements.

The detector array configuration of the FIP instrument maps to a single RFSoC device with the addition of a little RF processing to subdivide the total bandwidth into eight 2 GHz sections. The four detector signals are passed to a set of mixers that downconvert and split each 4 GHz signal into a pair of 2 GHz signals as shown in Fig. 11, which are interfaced to two RFSoC RF input channels at a time. All input signals are digitized in parallel. The RFSoC FPGA portion computes all spectra and generates the variable-frequency comb function that is sent back to the detector array. Detector bias and fluxramp modulation signals are also generated by the RFSoC and are sent to the detector array. The RFSoC also contains two different multicore processors on-chip, which can carry out all necessary software functions in the signal processing chain. These functions include input signal calibration, interfacing the instrument to the spacecraft via SpaceWire, tone tracking algorithm implementation,[5] and general-purpose board functions such as telemetry and health monitoring, limit checking, and any signal processing intelligence that is too cumbersome to implement in FPGA logic.
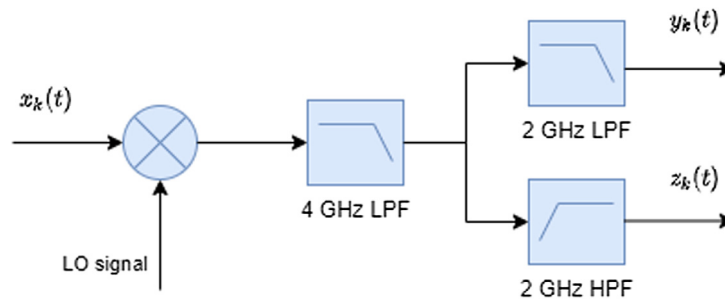

Fig. 11 Each of the four RF input signals $x_k(t)$ are mixed down to baseband using a 2-GHz LO and subsequently lowpass filtered to 4 GHz. The resulting signal is split into upper and lower spectral halves, which are acquired for subsequent signal processing, according to the frequency plan.

Utilization of the RFSoC, or any ASIC that has RF-Sampling data converters, simplifies the required radio-frequency and intermediate-frequency circuitry. For FIP, only a single RF-to-baseband downconversion stage is required, along with a two-channel RF filterbank with gain and filtering stages. The RF-to-baseband downconversion stage also incorporates any AC-coupling and anti-alias filtering required for interfacing the RFSoC input. Similarly, the RFSoC output stage requires baseband-to-RF upconversion, gain, and RF-combining circuitry.

3.2 Digital Spectrometer

A digital filter bank is a collection of related digital filters that share either a common input or a common output signal.[8] There are two types of filterbanks—synthesis and analysis. An analysis filterbank is used as the spectrometer processor for the FIP instrument in much the same way that the same type of filter bank was used in the Soil Moisture Active Passive Mission, launched in 2015.[9]

The filterbank consists of a polyphase finite-impulse response filter that is used to shape every frequency bin of the spectrometer. The polyphase filter employs a 50% overlap factor so that each analysis bin overlaps adjacent bins and no signal droop occurs between frequency bins. A standard fast Fourier transform is then applied to the polyphase-filtered data stream, averaged, and transmitted to the command and data-handling subsystem. The filterbank spectrometer operates in real-time, over the entire 4-GHz bandwidth of signal originating from each of HEMT amplifiers.

The digital spectrometer used for FIP signal processing is highly parallelized. The first level of parallelization is due to the detector array signals themselves being fed into eight parallel RF input ports of the RFSoC. All 7957 pixels, occupying a total of 16 GHz of bandwidth, are fed into 8 on-chip ADCs that are all sampling at 4 GSPS. The second level of parallelization comes from the ADCs themselves. The embedded data converters must demultiplex the high-speed 4 GSPS 12-bit data stream into 16 parallel streams of data clocked at the FPGA fabric rate of 250 MSPS. Since data are not re-interleaved, all algorithms that operate on the data must be developed to operate on the parallel data stream. Using the polyphase filterbank approach[8] in Chapter 4, parallel processing is straightforward, linear, and identical for every ADC input stream. Implementation of the polyphase filterbank spectrometer, comb function generation, and array signal processing functions are shown in Fig. 12.
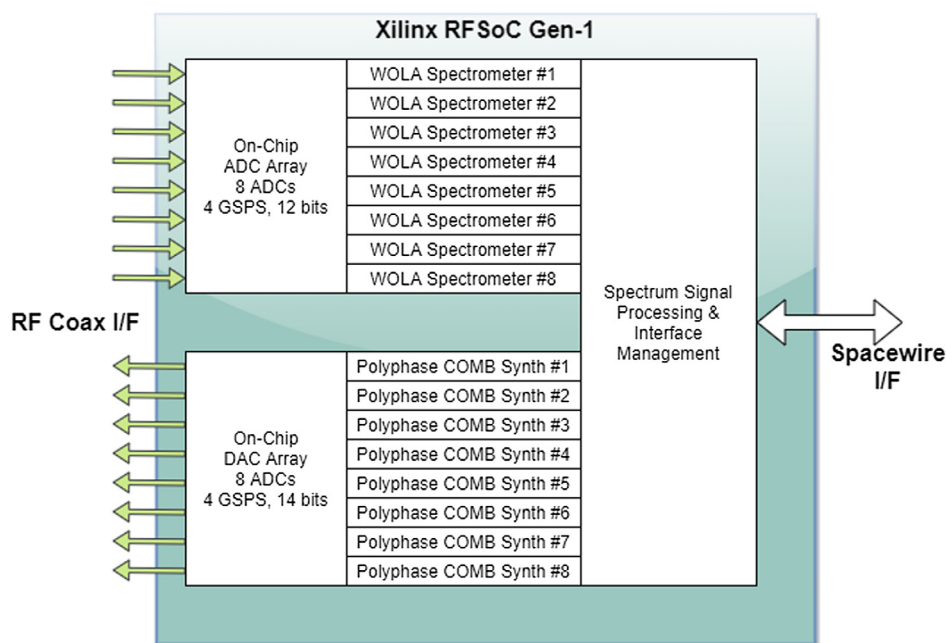

Fig. 12 Implementation of the polyphase filterbank spectrometer, comb function generation, and array signal processing functions implemented on the Xilinx RFSoC processor.

Currently, a hand-coded very high-speed integrated-circuit hardware description language (VHDL) implementation of our 50% weighted-overlap and add filterbank, with 1024 frequency bins per every 2 GHz of spectrum, utilizes 52% of the total logic of the RFSoC. This design is not yet optimized to use the majority of the DSP48 macros on the device; therefore, this utilization figure will decrease. Currently, our composite filterbank spectrometers, which is split into eight independent filterbank spectrometers, covers a total of 8192 frequency bins. This number will increase as the VHDL is optimized for performance.

3.3 *FIP Data Rate*

The primary output data product of the FIP instrument is a vector of 7957 12-bit numbers corresponding to the comb frequency amplitudes that are modified by the TES or MKID resonators. The signal processor produces 300 of these per second to maintain a 150-Hz scientific bandwidth. Therefore, the output data rate is the product of these quantities, or 7957 amplitudes × 300 Hz readout × 12 bits/amplitude = 28.7 Mbps. A 12-bit resolution, corresponding to a 72-dB dynamic range for each detector value, is sufficient to capture the detector's photon noise-limited dynamic range.

4 Future Work

The introduction of the RFSoC by Xilinx in 2017 had a monumental impact on digital signal processing systems worldwide and influenced the design of the FIP readout subsystem. The RFSoC is a single-chip solution—meaning that only a single RFSoC chip is needed to excite, read out, control, and process all signals required for detector array operation.

However, the major caveat is that, currently, the RFSoC is not radiation-tolerant, nor does Xilinx have immediate plans to make a radiation-tolerant version of this part. Therefore the RFSoC cannot be used in the final flight build for the FIP instrument or any spaceflight instrument for the time being unless a fault-tolerant approach for using them is developed. For ground and airborne instruments, the RFSoC is the most efficient part to use from a size, weight, and power perspective, but for space use, the RFSoC cannot be used without some method of fault-tolerance to protect the device against radiation effects.

As a development platform, however, the RFSoC enables the entire FIP instrument to be built, and it would reach what NASA calls a TRL-4,[10] which means that the development will work in the lab environment. The advantage here is that FIP, as an entire instrument, can be be developed efficiently, with a RFSoC-based readout electronics as its readout algorithm development and testing platform. As the instrument matures, the readout electronics subsystem could be swapped out for another one that does have radiation-tolerant parts. All of the same interfaces to the detector system and the data interface to the spacecraft can remain the same.

For FIP to operate as a spaceflight instrument at TRL-6, the unit must meet all space environmental requirements, including temperature and radiation. All DSP algorithms could be developed on the RFSoC and ported to radiaton-tolerant FPGAs, such as the Kintex Ultrascale FPGA, also from Xilinx.[11] The disadvantage of this approach is that external signal data converters would necessarily need to be used, thus significantly increasing the PCB size and number, cost, complexity, and power. Since the FIP instrument uses 16 data converters internal to the RFSoC, all of these would have to be external to a device such as the Kintex Ultrascale. External, monolithic, and radiation-tolerant data converters are currently available at the same sample rates as the internal data converters of the RFSoC. However, since they are external, they require very high-speed digital interfaces to the FPGA, resulting in multiple complex PCBs needing to be implemented versus a single RFSoC-based PCB. It is estimated that a Kintex FPGA can only support a total of four external data converters (2 ADCs and 2 DACs) using high speed serial data interfaces such as JESD204B.

We estimate a board like this requiring 30 W and a total of four PCBs like this needing to replace a single RFSoC-based board. A system built using this approach could be built today and meet the requirements of a FIP flight instrument, but using significantly more mass, power, and volume than a functionally equivalent RFSoC-based system.

To estimate power, as a reference, Abaco Systems was one of the first commercial vendors to make an RFSoC-based PCB, and they estimate 50 W of total power consumption for the entire system. This is a conservative estimate. To compare against a conventional FPGA system with external data converters, one can estimate ~1 W per GHz of sample rate in total power utilization, also taking into account the JESD204B interface to the FPGA. For a Kintex-based system, we require at least 4 GHz of sample rate for DACs and ADCs, and only 4 of each data converter can connect to one Kintex FPGA. Therefore we have 8 W of power used for DACs and 8 W for ADCs. In addition, the FPGA itself on this PCB would utilize a conservative 20 W, assuming a nearly full device, with digital logic clocking as quickly as possible. The big drawback of such a system is that a total of 4 PCBs, each with four data converters and 1 FPGA, would be required to have to same signal processing functionality of a single RFSoC-based board. Coincidentally, Abaco Systems actually notes this fact on their website with an advertising animation explaining the same advantage. Clearly, this is a strength of using the RFSoC for FIP signal processing.

A notional estimate summarizing the power requirements of a TRL-6 readout versus a TRL-5 readout based on the RFSoC is given in Table 1. A standard power loss of 15% due to power conversion inefficiency that is typically seen in spaceflight electronics, and 10% margin for supporting electronics on the same PCB were assumed in the estimations for each subsystem.

Another approach, instead of using a high TRL-level but high-power consumption readout for FIP, would be to use ASIC spectrometers instead of FPGAs and data converters. This is the most power-efficient but most costly option since custom chips would be designed from scratch. Commercial vendors such as Alphacore and Pacific Microchip are entering the market now with such offerings, but they are severely limited since their devices are only spectrometers. In addition, they present a similar radiation risk as the RFSoC since none of these devices have reached TRL-6 yet. ASIC spectrometers wouldn't solve the readout problem entirely. FPGAs would still be required to generate the necessary comb signals to excite the detector array and interface the detectors, and would also be needed to interface the spectrometer ASICs themselves and tie the entire electrical systems architecture together.

Using the RFSoC as a ground-based development platform, while commercial electronics matures for spaceflight use, is a prudent approach since the FIP as a system is optimized functionally. All of the FPGA designs are portable between RFSoC and any other device, and the readout system is modular and linear so that it is FPGA-agnostic. The RF frequency plan can remain the same.

Table 1 Power estimation for the digital (non-RF) portion of the FIP readout electronics. Two options are presented—a TRL-6 conventional readout versus TRL-5 RFSoC-based readout.

Device	TRL-6 conventional rad-tolerant readout electronics		TRL-5 RFSoC-based readout electronics	
	Quantity	Estimated power (W)	Quantity	Estimated power (W)
FPGA	1	20	1	50
ADCs (TI 6.4 GSPS)	2	8	0	0
DACs (E2V 8 GSPS)	2	8	0	0
Number of PCBs required	4	—	1	—
Power subtotal	—	144	—	50
Overhead power (10%)	—	14.4	—	5
Power loss due to inefficiency (15%)	—	2.16	—	0.75
Total estimated power	—	**160.56**	—	**55.75**

Note: Bold emphasizes total estimated power.

5 Conclusion

The technology roadmap for detector readout for OST is both realistic and compelling. Although it is currently based on using the revolutionary TRL-5 RFSoC technology that is only commercial and not space-qualified, there are still several paths that lead to TRL-6 and beyond given investment in this approach. At a cost of about 160 W and a box with 4PCBs, the FIP readout electronics could be built and flown in space today with available radiation-tolerant parts. Using the RFSoC reveals that, in the future, it will be feasible to do the same job with only 1 PCB and 55 W or less. If Xilinx decides to make the a radiation-tolerant version of the RFSoC in the near future, then FIP immediately benefits from it and jumps to TRL-6 with the most efficient FPGA-based approach to readout. If not, there are still compelling ASIC spectrometer chips that can be combined with smaller, radiation-tolerant FPGAs on the same PCB that can lead to electronics solutions that are increasingly power-efficient. The industry is already heading in a direction that makes all of the aforementioned approaches technically sound and programmatically reasonable. As a result, the FIP instrument is on track with its technology roadmap and will lead to unprecedented science that takes advantage of all of the various investments and significant gains that are happening now in commercial and government technology development.

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