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Developments of Laboratory-Based Transition-Edge Sensor Readout Electronics Using Commercial-Off-The-Shelf Modules

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Abstract

We are developing lab-based readout electronics for Transition-edge sensors (TES) using commercial-off-the-shelf (COTS) modules. These COTS modules are advantageous since they increase development speed and keep the cost low. We have developed these electronics to support both non-multiplexed and time-division multiplexing (TDM) readout systems. The system utilizes remote control via Ethernet, and the interface allows many types of measurements to be automated. With the TDM readout system, we have achieved 2.05 eV at 6 keV, 2.1 eV at 7 keV, 2.3 eV at 8 keV, and 2.8 eV at 12 keV with 2-column × 32-row multiplexing. We will be using this system in the characterization of detectors for the X-Ray Integral Field Unit (X-IFU) instrument on Athena. In this paper, we present an overview of the design and their performance.

Keywords Transition-edge sensor · Time-division multiplexing

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1 Introduction

At NASA Goddard Space Flight Center (hereafter Goddard), we are providing a kilo-pixel array of TES microcalorimeters for the X-Ray Integral Field Unit (X-IFU) of the European X-Ray Observatory Athena [1], and during the development, various types of other prototype arrays need to be characterized. These array sizes vary from a few tens to over three thousand pixels, and it is crucial to characterize them effectively and rapidly. We are therefore developing in-house readout electronics that can easily be interfaced with modern computers via Ethernet and remotely controlled to automate various types of measurements. These electronics are utilizing Commercial-Off-The-Shelf (COTS) modules to increase development speed and keep costs low. We have developed a readout system for non-multiplexed readout as well as time-division multiplexing (TDM) [2] readout. The non-multiplexed readout system supports readouts of up to three pixels and has one channel of function generator that can be used for complex impedance measurement. Most of the recent successful results of non-multiplexed readouts at Goddard were measured with this system. The TDM readout system consists of two separate electronics, row and column, and supports 40 rows and 4 columns. The number of columns is scalable by adding more column electronics to the system. With the TDM readout system, we have demonstrated a 2-column × 32-row TDM multiplexing and achieved 2.05 eV at 6 keV, 2.12 eV at 7 keV, 2.28 eV at 8 keV, and 2.84 eV at 12 keV. Here, we present an overview of the design and describe some of the technical details of these electronics and their performance.

2 Non-multiplexed Readout Electronics—TES Analyzer

The 'TES Analyzer' is an in-house made combined Digitizer and Function Generator (Fig. 1), and it can be used for various TES measurements, such as acquiring triggered pulse data stream records, collecting noise data, taking I/V characteristics, and making complex impedance measurements, with a use of an external flux locked

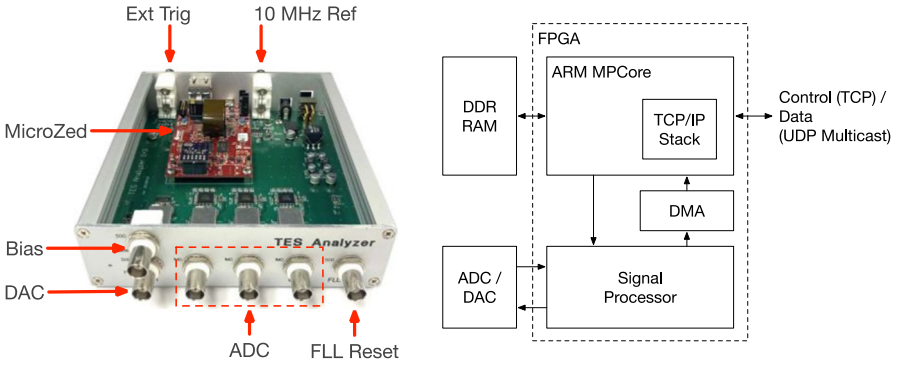

Fig. 1 The TES Analyzer hardware (Left) and block diagram (Right) (color online)

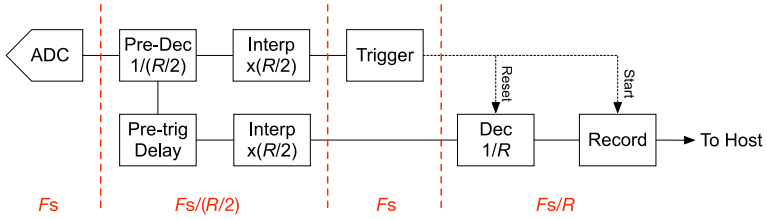

Fig. 2 Block diagram for the signal processor in the FPGA firmware, where *F*s is the sampling frequency and *R* is the decimation rate. The solid line shows the data flow, and the dashed line shows the timing signals

loop, such as the Magnicon XXF-1. It consists of three 14-bit ADC (AD9240) and one 14-bit DAC (AD9764), all running at 10 MS/s. There is an additional 16-bit slow auxiliary DAC intended for a field coil or a bias for a TES or a superconducting quantum interference device (SQUID). The input and output ranges for the fast ADC and DAC are ± 1 V with an offset adjustment of ± 2 V (ADC) and ± 4 V (DAC), and the output range for the slow DAC is ± 2 V. There is an analog 40 dB attenuator for the fast DAC that is optionally turned on to generate a small-amplitude sinusoidal wave for complex impedance measurements. Additionally, there is an isolated 10-MHz reference clock input/output, an external-trigger input/output port, and a flux-locked loop (FLL) reset signal port designed for integration with the Magnicon XXF-1.

The ADC and DAC are interfaced to a Field Programmable Gate Array (FPGA), which is a commercial module, the Avnet MicroZed with a Xilinx XC7Z020. Figure 1 shows the simplified hardware block diagram. The ADC sampled data is processed in a signal processor block in the FPGA, which mainly performs triggering, decimation (change of sampling rate), and recordization. Figure 2 shows the block diagram of the signal processor. After digitizing it splits the input stream into two, one stream for triggering and the other for recordization. Both streams are then low-pass filtered by a combination of decimation and interpolation using cascaded integrator-comb (CIC) filters [3]. The decimation rate is kept lower than the final decimation rate by a factor of two so that the final signal will not be over low-pass filtered. The filtered stream for triggering is then triggered either by a level trigger or a slope trigger. When a trigger is fired, two timing signals are generated, a reset signal for the decimation CIC filter and a start signal for recordization. Because the triggering is carried out at the native sampling frequency and the final decimation is aligned to the triggering timing signal, the trigger jitter for the final record is kept small so that a trigger-jitter correction [4] can be avoided in data analysis.

The TES Analyzer runs a command server on one of the hard-core processors in the FPGA and accepts Transmission Control Protocol (TCP) socket connections. The triggered record data are sent to the processor via direct memory access (DMA) and then transferred to a host computer using a User Datagram Protocol (UDP) multicast. We have also developed a host-side application to control the hardware and plot the data. Since the network-based interface is very simple and a low-level interface library is also developed, it does not limit the use of the TES Analyzer to the

existing software application, and it can be easily interfaced by any custom-made software. This enables us to easily develop an automated measurement for application for characterizing a large number of TES pixels. We have been using the TES Analyzer for our TES measurements, and the recent non-multiplexed readout results were all taken using this. For example, our best energy resolutions of 1.58 eV at 5.9 keV [5] and 0.25 eV at 3 Ev [6] were taken using this TES Analyzer.

3 TDM Digital Electronics

The TDM Digital Electronics consists of two boxes of electronics: Row and Column. At a minimum, one box each for row and column functions is needed to run the system, and an additional column box can be added to add more TDM columns. These electronics are designed to be used with the NIST analog front-end and cold electronics [7].

The row electronics, shown in Fig. 3 (*Left*), provides TDM row switching signals up to 40 rows with 10 HDMI connectors. The switching voltage is configurable from 0 to 2 V, which is provided by a single 16-bit DAC that is shared by all rows. For each row, a row-switching pulse for SQUID is generated by a CMOS switch (ADG719), which switches between ground and the voltage generated by the DAC. The switching signal for the CMOS switches is generated in an FPGA, which is on a MicroZed module. Any switch can be simultaneously turned on, which enables the use of two-level switches [8]. We have measured a ~ 20 ns of transient time for a 1 V square-pulse across a 2 k-ohm resistor.

In addition to the generation of the switching signal, the Row electronics generates the 100 MHz reference clock using a crystal oscillator and distributes it to the column electronics. It also generates the 245.76 MHz master clock using a phase-locked loop (PLL) and the FPGA uses this clock to generate the row switching

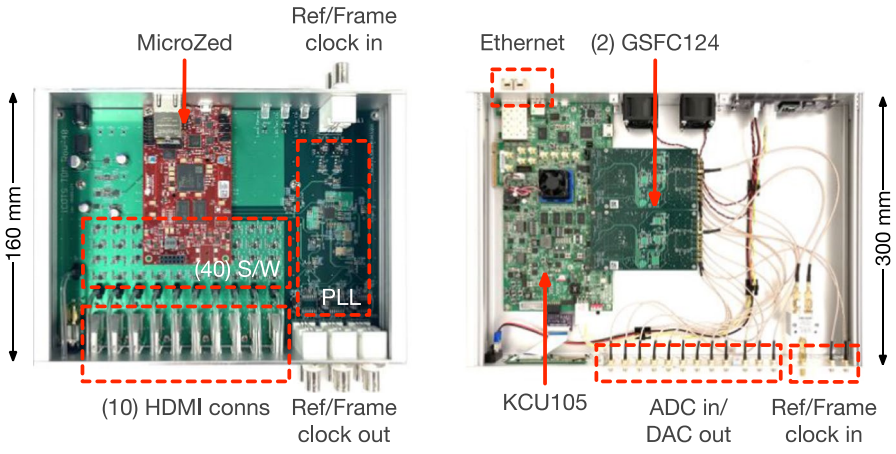

Fig. 3 The TDM row electronics using MicroZed (Left) and the TDM column electronics using Xilinx KCU105 (Right) (color online)

signal for the CMOS switches. In addition, the FPGA generates a frame clock, which is a timing signal to mark the beginning of the first row and distributes it to the column electronics.

The column electronics is at the heart of the system, and it performs TDM demultiplexing and generates SQUID feedback signals for both a front-end SQUID and an amplifier SQUID. For each column, it uses one ADC for an error signal input and two DACs for SQUID feedback signal outputs. We have developed the prototype hardware consists of a Xilinx VCU118 FPGA evaluation board and two in-house developed ADC/DAC daughter cards, GSFC124. The GSFC124 deploys a dual-channel 14-bit 250MS/s ADC (ADS62P49) and two dual-channel 16-bit 800MS/s DACs (DAC3283), and thus two GSFC124 cards allow a 4-column TDM system. The reference clock from the row electronics is fed into the GSFC124 cards after being split into two and used to generate the master clock using a PLL. The ADC/DAC sampling rate is at this master clock frequency.

The firmware functionality of the column electronics is similar to the existing NIST electronics [7] with a few exceptions. One is the pulse shaping, which is a digital low-pass filter that can be optionally applied to slow down the rise time and fall time of pulse-wave-like feedback signals to reduce overshoot and ringing in the signal lines. The other functionality is the scope mode, which processes the native ADC sampling data and transfers triggered data to the host computer. This functionality is like having an oscilloscope mode for signal visualization and makes it easier to tune the TDM timing parameters as well as to diagnose high-frequency noise. For both TDM de-multiplex signal and the scope mode signal, signal is triggered in the FPGA and transferred to a host computer using a UDP multicast, and unlike the TES Analyzer there is a hardware UDP multicast module in the FPGA fabric, and it uses a separate Ethernet port from a control Ethernet port.

As with the TES Analyzer, each row and column box run a stand-alone command server and can be controlled through a TCP network connection from the host computer. The TDM readout is currently controlled by our own application, but it can be also controlled from any custom-made software for the automation of various measurements.

Figure 4 shows the co-added Mn-Kα, Co-Kα, Cu-Kα, and Br-Kα energy histograms that are taken with the TDM electronics with the 2-column × 32-row multiplexing. We measured ΔE_{FWHM} of 2.05 ± 0.02 eV for Mn-Kα, 2.12 ± 0.02 eV for Co-Kα, 2.28 ± 0.02 eV for Cu-Kα, and 2.84 ± 0.02 eV for Cu-Kα, which are comparable to the results measured using the existing NIST TDM electronics [9]. The FPGA board has been recently replaced with a Xilinx KCU105 for a production system, shown in Fig. 3 (*Right*), and we will use this system to characterize the detectors for the Athena X-IFU instrument.

4 Summary

We have developed non-multiplexed and TDM readout systems using COTS modules. The use of the COTS modules helps to increase the development speed while reducing the cost. With the non-multiplexed readout system, we have

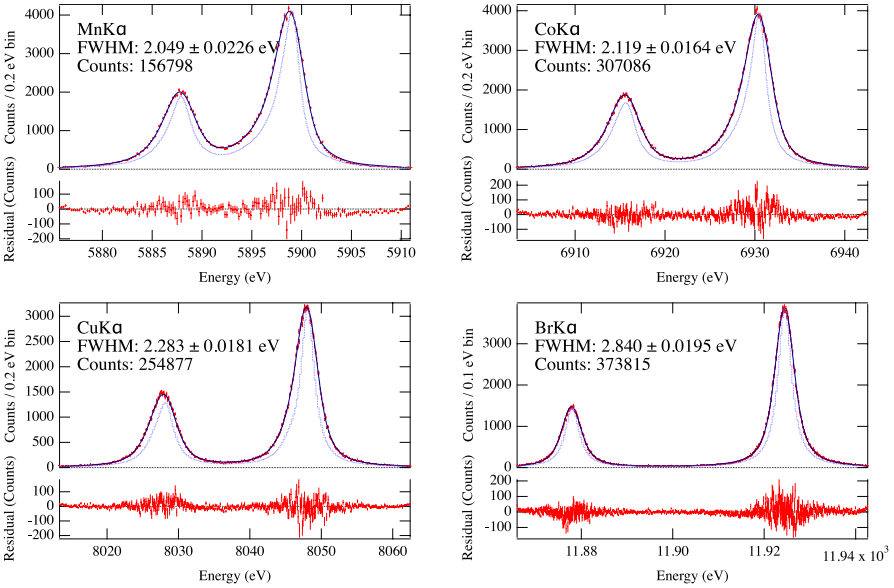

Fig. 4 The co-added Mn-Kα (Top Left), Co-Kα (Top Right), Cu-Kα (Bottom Left), and Br-Kα (Bottom Right) energy histograms taken with the TDM electronics with 2-column × 32-row multiplexing. The red dots are the data points, the light blue lines are the natural line shapes, and the dark blue line is the fit to data. The best fits give $<\Delta E_{\mathrm{FWHM}}> = 2.05 \pm 0.02$ eV@6 keV, 2.12 ± 0.02 eV@7 keV, 2.28 ± 0.02 eV@8 keV, and 2.84 ± 0.02 eV@12 keV. (color online)

measured 1.58 eV at 5.9 keV and 0.25 eV at 3 eV. The TDM readout system has measured 2.05 eV at 6 keV, 2.12 eV at 7 keV, 2.28 eV at 8 keV, and 2.84 eV at 12 keV with 2×32 multiplexing, and these are comparable to the results using the conventional readout system.

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