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Design and Fabrication of Nanostructure for Mid-IR Antireflection Surface Texturing Applications

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ABSTRACT

Reduction of unwanted light reflection from a surface of a substance is very essential for the improvement of the performance of optical and photonic devices. Anti-reflection (AR) surface textures can be created on the surface of lenses and other optical elements to reduce the intensity of surface reflections. AR textures are indispensable in numerous applications, both low and high power, and are increasingly demanded on highly curved optical components.

Nanofabrication involves the fabrication of devices at the nanometer scale. In this work, we used nanofabrication to design and fabricate nanostructures of squares and hexagons of different spatial pitch and gap width in Gallium Arsenide (GaAs). These structures have a gap of 300nm, 400nm, and pitch of 900nm, 1000nm and 1100nm. The fabrication process involves solvent cleaning, deposition of silicon oxide, soft and hard bake, photolithography and development. Both wet and dry etching were used to fabricate the expected structures. Results from scanning electron microscopy (SEM) to examine the shapes of the fabricated arrays are presented in this study. By combining dry and wet etches, we obtained the desired shapes and depth of hexagons and squares with rounded edges. We report detailed fabrication processes and their corresponding results at each step.

Keywords: Anti-Reflection, Nanostructures, Nanofabrication, Dry etching, Wet etching, Textures, Photolithography, Arrays

1. INTRODUCTION

The anti-reflective (AR) surface was discovered during the time of Lord Rayleigh in the late 19 centuries. [1] He tested some slightly tarnished glass and new clean pieces to transmit light from both surfaces and found out the former transmits more light than the latter. This was because the refractive index of the tarnish between air and glass resulted in the reflection exhibited by the two interfaces was less than that of the clean air-glass interface. Along with that, there are many other ways to minimize reflection. Suppressing reflections from optics and windows has long been accomplished by depositing multiple thin layers of dielectric materials onto each external surface of the window or optic. AR surface made of multiple discrete layers of non-absorbing materials can exploit thin-film interference effects to reduce the reflectance and improve the transmittance. [2] Reducing optical reflection from surfaces is vital to numerous applications in optics like in display screens [3], solar cells [4,5], and photodetectors. Multi-layer Interference, where an alternating layer of low index material with high index material combined to give very low reflectivity over a broadband range of frequency. [6] The main drawback is that these layers are getting thicker at longer wavelength and become easier to crack and less reliable, which makes this technique less attractive for mid-IR applications; although, it can obtain the reflectivity as low as 0.1% at a single wavelength.

Various other research was conducted to reduce the reflection from optical surfaces. Joseph Fraunhofer, who showed that acid etching of certain glass surfaces substantially reduced the reflection [6]. Bernhard models the conical protuberances found on the corneas of moths' eyes as a graded refractive-index region. Wilson and Hutley, describe artificial moth-eye surfaces produced by recording, in a photoresist, interference fringes generated at the intersection of two coherent laser beams. [7] In order to produce AR properties for a wide range of incidence angles and wavelengths, surface texture techniques are utilized to produce subwavelength structures on the interfaces. Among the subwavelength structures,

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moth-eye nanostructure interests many researchers which is inspired by nature. Moth's eye has unusual property since their surfaces are covered with the natural nanostructured film which eliminates reflection. [8] Moth eyes bio mimic the anti-reflective ability which makes it more difficult for their predators to find them. Their eye structure consists of a hexagonal pattern of bumps which are smaller than the wavelength of visible light, so the light sees the surface as having a continuous refractive index gradient between air and the medium, which decreases the reflection. [9] The moth-eye nanostructure is one of the most promising structures which exhibits high transmission and low reflectivity with a wide range of wavelengths. When we are more concerned about applications like surface adhesion, minimal surface preparation, and environmental tolerance, moth-eye structure is preferred when compared with traditional thin-film AR surfaces. Hence, these nanostructures can provide better performance, less cost and able to withstand under the harsh environmental condition and abrasive environment for military operations.

To obtain these nanostructures, a large number of fabrication technologies such as nanoimprint lithography, electron-beam lithography (EBL), laser interference lithography, has been proposed and developed in the past. The subwavelength scale AR nanostructures in silicon were fabricated using a wafer-scale nanoimprint technique. Toyota et al. fabricated an AR surface with sub-wavelength structures on a fused silica substrate with the help of the etching mask formed by an EBL and lift-off process. [10] Zhang et al. fabricated the array of nanostructures using roll to roll UV-Nanoimprint lithography. [11] Xu et al. [12] obtain moth-eye nanostructure arrays on a surface of a silicon wafer using direct six-beam LIL to improve the AR performance of the material surface and the feasibility of this method was validated to fabricate cross-scale moth-eye structures for AR applications by theoretical and experimental results. Yoshiaki et al. produced tapered gratings with a 150 nm period and a 150 nm deep groove on a glass substrate by EBL. [13] The above technologies are feasible for obtaining the nanostructures on a small scale but are not suitable for commercialization which requires low cost, no complex setup, high mass production.

To overcome the limitations of the fabrication technologies above, we designed and fabricated the nanostructures of squares and hexagons pattern on gallium arsenide using contact photolithography. The technique requires no complex setup, low cost and has high throughput. In this work, squares and hexagons have a gap of 300nm and 400nm between the neighboring pattern while the spatial pitch is of 900nm, 1000nm and 1100nm. The paper is organized as follows…First, nanostructures are designed using any drawing tool like AutoCAD or L edit and photomask is fabricated which can be reused to produce the structures on GaAs. Then, the fabrication steps to obtain the nanostructures and their results are discussed in detail. Scanning electron microscopy (SEM) results are shown and pattern shapes obtained are closely examined. Finally, issues faced during the fabrication processing, if any are resolved.

2. DESIGN AND PHOTOMASK FABRICATION

2.1 Design

The first and foremost step is to design a nanostructure that can achieve transmission as high as possible. There are many methods and models which are instrumental to find the design of these structures but the basic is the one which was inspired from moth's eye structures.
Our design consists of 12 windows each of 0.5*0.5 cm where 6 windows contain the squares pattern and the other six for hexagons pattern. The gap between the neighboring pattern is 300nm and 400nm with a pitch of 900nm, 1000nm and 1100nm. Fig 1 and 2 shows the hexagons and square patterns of different pitch and gap designed in AutoCAD.

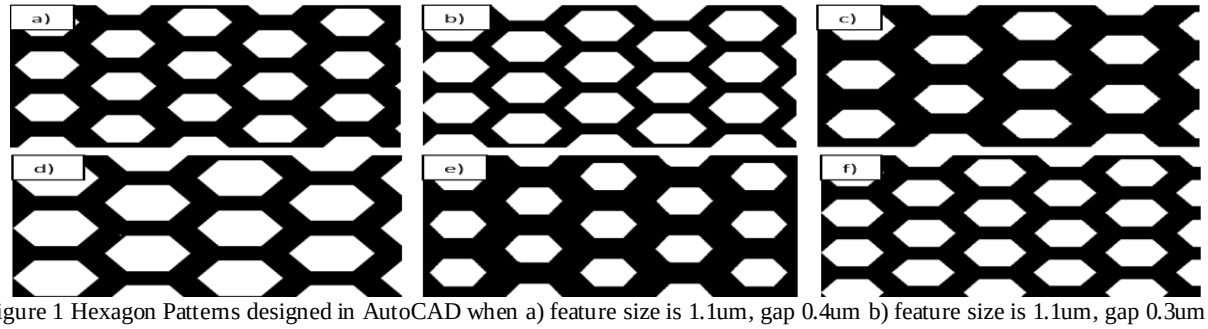

Figure 1 Hexagon Patterns designed in AutoCAD when a) feature size is 1.1um, gap 0.4um b) feature size is 1.1um, gap 0.3um c) feature size is 1.0um, gap 0.4um d) feature size is 1.0um, gap 0.3um e) feature size is 0.9um, gap 0.4um f) feature size is 0.9um, gap 0.3um

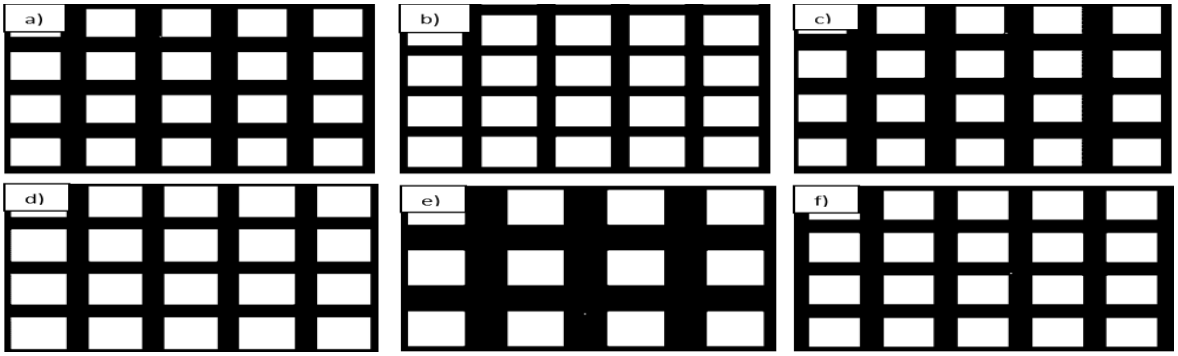

Figure 2 Square Patterns designed in AutoCAD when a) feature size is 1.1um, gap 0.4um b) feature size is 1.1um, gap 0.3um c) feature size is 1.0um, gap 0.4um d) feature size is 1.0um, gap 0.3um e) feature size is 0.9um, gap 0.4um f) feature size is 0.9um, gap 0.3um

2.2 Photomask Fabrication

A photomask is a quartz or glass substrate, coated with an opaque film, which is designed to optically transfer patterns to wafers or other substrates. The pattern (squares and hexagons) information is created in the AutoCAD tool. The design is reformatted into internal CAD format and transfer to E-beam writer which exposes the design onto the photomask substrate. Photomask fabrication involves many steps such as data preparation, exposure, chrome process, etching, stripping and photomask cleaning. [14] Data preparation translates the set of designs and layers onto the set of instructions that photomask writers use to generate the physical mask. The squares and hexagons are processed into the Gerber data format and design is delivered to photomask data preparation in DXF or GDSII format which is binary data format represents planar geometric shapes, labels and/or other information of the design. The exposure will transfer the pattern designed in AutoCAD onto the selected photomask. The substrate has chrome on one side and is placed for writing and imaging in the chrome process step. The light-sensitive particles on the resist absorb the light and this creates a latent image in the photoresist layer. With developing the sample in the developer, the resist from unexposed parts becomes soften and dissolve out the mask layer. The required pattern will be obtained on photomask with the conclusion of this step. Etching will remove the chrome part that is not required which is outside the design area and stripping will strip out the remaining photoresist from the photomask. Finally, the photomask surface is cleaned with acetone/methanol and is ready to be used for optical lithography or UV lithography. Figure 3 shows the 6-inch photomask we provided design and fabricated by mask vendor using e-beam lithography.

Figure 3 Fabricated Photomask with 12 windows of 0.5*0.5 cm each, the array of square patterns are arranged uniformly in 6 windows while other 6 windows contain an array of hexagon patterns

3. FABRICATION OF NANOSTRUCTURES

In order to obtain the nanostructures on gallium arsenide, a certain fabrication process needs to be followed. The process involves steps like solvent cleaning, photoresist spinning, soft and dry bake, exposure and development, dry and wet etches to get the desired structures onto the substrate. The fabrication was performed in cleanroom class 10 and 100. The process assumes that a bare gallium arsenide wafer is used and outlines all the steps below to fabricate the design.

3.1 Solvent Cleaning

The most important step in fabrication is cleaning the wafer. Wafers usually become contaminated simply when exposed to the air, which contains a high degree of organic particle contaminants. The contaminants strongly make bonds with the wafer surface due to strong electrostatic force and the surface becomes rough. The fabricated design on that kind of surface will not be efficient. In order to get the design properly on the surface, the wafer must be completely free of contaminants. The solvent clean will remove the oils and organic residue from the surface of the GaAs wafer. Solvents leave residue on the surface of the wafer even though it removes the contaminants. For this reason, the two-solvent method is implemented, one with acetone and then with the methanol to get the clean surface. If the surface is still contaminated, it can be further cleaned in hydrofluoric acid (HF). HF is a dangerous chemical, so special caution must be taken during this step.

3.2 Deposition of Silicon Oxide

This step involves depositing a thin layer of silicon dioxide on the GaAs wafer. The layer will act as a protective layer for the gallium arsenide surface. Thus, it acts as a passivation layer. To grow the oxide layer on top of the surface, we used the plasma-enhanced chemical vapor deposition (PECVD) system. PECVD is a chemical vapor deposition process used to produce a thin film on wafer/substrate generally at a temperature of 200-300 degrees Celsius. In the process, deposition is achieved by introducing reactant gases between parallel electrodes and the capacitive coupling between the electrodes excites the reactant gases into plasma. The plasma so formed produces a chemical reaction and the reaction result was being deposited on the substrate. [15] PECVD is commonly used over CVD because the temperature at which the substrate was heated is around 200 degrees Celsius which is less as compared to 400 degrees Celsius with CVD. If we subject to increase the temperature above 300 degrees for GaAs, the wafer could get degraded. The lower deposition temperatures are vital in many applications where CVD temperature damage the devices being fabricated. We deposited 2500 Angstrom of oxide on the surface and since the oxide rate was 720 angstrom per minute, we allow the wafer in the system for 4 minutes to get the required thickness of the oxide layer on the surface. After the deposition was done, the color of wafer changes to violet-blue color. Figure 4 (middle) shows the violet-blue color silicon dioxide on gallium arsenide surface.

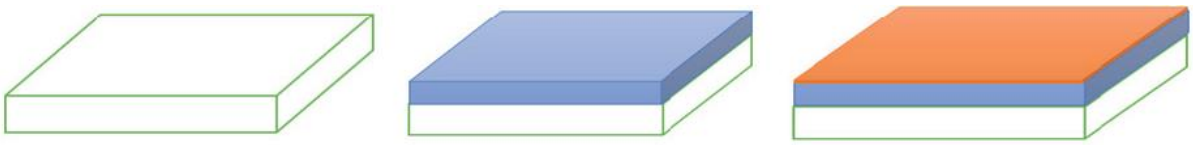

Figure 4 clean Bare GaAs wafer (left), Oxide growth on GaAs, Violet color represents SiO2 (middle), HMDS and photoresist spinning (right)

3.3 HMDS and Photoresist Spin

The adhesiveness of resists on different substrates varies. Many substrates like silicon, silicon nitride show generally good adhesion features. However, on substrate-like gallium arsenide, gold or silver, adhesion is low. To adhere to the uniform resist on the surface, the adhesive promoter is required. There are many useful adhesive promoters like hexamethyldisilazane (HMDS), diphenylsilanediol-derivatives, Ti-Prime. Since HMDS is well suited for gallium arsenide, we used HMDS. HMDS binds to water-free surfaces via its Si-atom to the oxygen-atoms of oxidized substrate accompanied by the release of ammonia. The non-polar methyl groups provide a hydrophobic surface with good resist

adhesion and good wetting. This makes the GaAs surface dehydrated. We spin the HMDS at the speed of 3000 revolutions per minute (RPM) on a GaAs wafer.

A few ml of photoresist is spread on the wafer and spin at the rotational speed of several 1000 RPM. Depending upon the speed, the thickness of the photoresist is deposited on to the wafer and depending on which series of photoresist we used, the thickness to spin speed varies. In our processing, we used dilute S1805 (3 parts of posit thinner with 1 part of photoresist) photoresist of microposit S1800 series. Figure 4 (right) shows the photoresist (orange color in figure) spin on the surface. S1805 is a positive photoresist meaning, a portion of the photoresist that would be exposed to the light becomes soluble to the photoresist developer while the unexposed portion of photoresist remains insoluble. We spin at the speed of 4000 rpm and get a thickness of around 500 Angstrom. The principle of spin coating is that because of centrifugal force, the dispensed resist spreads uniform resist film of desired thickness and excess resist is spun off the edge of the wafer. At the same time, a part of the solvent evaporates from the resist film, so that its thinning stopped on the one hand and on the other hand, the resist film becomes sufficiently stable to suppress its elapsing during the handling of the wafer after coating. The film of resist on the surface is very smooth, the thickness can be adjusted accurately, and the entire process is reproducible.

3.4 Soft Bake

Right after the coating of resist on the GaAs wafer, we need to soft bake the wafer on the hot plate at 100 degrees Celsius for 2-3 minutes. After the photoresist deposition, the resist film contains the solvent concentration which must be driven out by soft bake. Soft bake will improve the resist adhesion and minimizes the dark erosion during the development step. It is important to note that the soft bake too hot or too cool for a longer time, can cause wafer contamination or decompose a fraction of photoactive compounds in photoresists and as a result, reduces the development rate. So, to avoid these problems, soft bake should be done with optimal temperature and for the optimal time.

3.5 Photolithography exposure and development

Lithography is the cornerstone of micro and nanotechnology fabrication. There are many lithography methods that we can use. For this process, we are using the optical lithography which refers to the lithography technique in which geometric pattern from photomask is transferred to the photosensitive chemical photoresist on the substrate using ultraviolet (UV) light. A patterned glass photomask having a layer of chrome is held on the top of the GaAs wafer. A source of UV light exposes only the areas of the UV light-sensitive photoresist layer that are not covered by chrome. Since the photoresist we used, is a positive one, so the areas that were exposed to light becomes soluble in the developer. The exposure is done under yellow light (cleanroom class 10) for 7-8 seconds to avoid unwanted exposure of UV sensitive photoresist.

Once exposed, development is important because we won't be able to see the pattern on the GaAs wafer. There are many developers out in the market, but the specific developer is used for certain photoresists. We used dilute Az400K (one part of a developer with 3 parts of DI water) developer for positive photoresist because our concern was towards high sensitivity rather than high contrast. To get high contrast, 4 parts of DI water is mixed with 1 part of the developer. Az400K is potassium based and is buffered to maintain the uniform pH and to provide process stability and developer bath life. It is an odorless, aqueous, inorganic, alkaline solution, free of phosphates and sodium. We dipped the wafer in the developer for 10-15 seconds before we were able to see the square and hexagon patterns. The development time varies depending upon how thick the photoresist is, and how narrow the design needs to see on the wafer. Figure 5 (left) shows the pattern of squares and hexagons after photolithography and development.

Figure 5 U.V exposure and Development (left), RIE dry etching and wet BOE etching (middle), Final patterns on gallium arsenide after photoresist removal (right)

3.6 Hard Bake

When we successfully develop the patterns on the GaAs wafer, wafer was hot baked at the temperature of 130 degrees Celsius for 5 minutes and cool down the wafer for 2 minutes at room temperature which will suppress the cracks, if any from the wafer. A hard bake after the development increase the chemical, the physical and thermal stability of resist structures for next steps such as dry and wet etching. A hard bake after the development can increase the resist adhesion for subsequent wet etching. Chemical bonds between the substrate and resist become strong giving high adhesiveness.

3.7 Dry and wet etching

The next step in the processing is to etch away the silicon dioxide from the wafer. To etch away, we used the reactive-ion etching (RIE) technique, in which there are 3 available gases such as O2, CHF3, SF6. We used SF6 to successfully etch away the SiO2. RIE is an anisotropic method, meaning the etching would be non-uniform in a different direction. The pressure was fixed at 250mTorr and power 100Watt. Since the etching rate of RIE is 230 angstrom per minute, we kept the wafer for 5 minutes to etch the 1000 angstrom of silicon oxide.

Unlike dry etching, wet chemical etching is an isotropic process (uniform etching in all directions) and will remove the remaining silicon dioxide by undercutting from the GaAs wafer. A buffered oxide etch (BOE) also known as buffered HF or BHF is used to etch the thin film of SiO2. The etching rate of BOE is 40 angstrom per second and frequently checking the wafer under the high-resolution microscope is significant during this step.
Both dry and wet etches will provide the desired squares and hexagons pattern with rounded edges on the gallium arsenide wafer. Figure 5 (middle) shows the silicon dioxide is etched and the pattern are obtained after cleaning the Photoresist from the surface (right). Figure 6 shows the final patterned Gallium arsenide wafer.

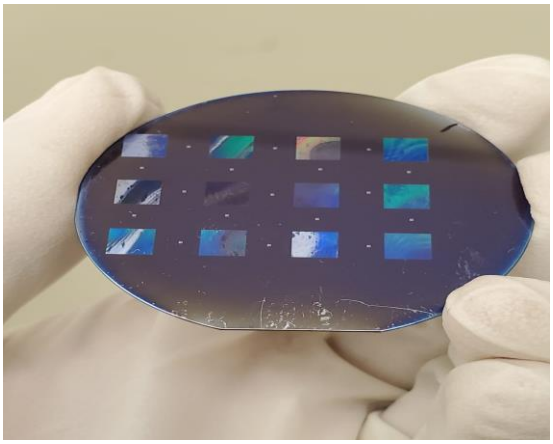

Figure 6 Final GaAs wafer with squares and hexagons pattern on the surface after fabrication

3.8 Issues faced

There were numerous problems that hinder our progress in obtaining the desired structures. When the surface was etched and observed under the scanning electron microscope (SEM), some areas in squares or hexagons window has not been etched to enough depth. It is shown in Figure 7. The under etching effect is because of newton's rings created due to the non-uniform gap created unintentionally between the photomask and the wafer during the UV light exposure. These are interference patterns formed by the reflection of light between the two hard surfaces as there is a slight gap of few nano or micrometers between these surfaces. The interference results in a pattern of bright and dark bands sometimes called interference fringes are observed on the surface. These bright and dark fringes are because of constructive and destructive interference. Constructive interferences are formed when the path length difference between the two rays reflecting on the surface of the photomask is an odd multiple of half wavelength, the troughs, and peaks of reflected waves coincide and result in a greater light intensity which corresponds to the bright fringes. On the other hand, when the path length difference between the two rays reflecting on the surface of photomask is an even multiple of half wavelength, the reflected waves will be out of phase, and hence waves will cancel each other resulting into weaker light intensity which corresponds to the dark fringes are refer as destructive interferences.

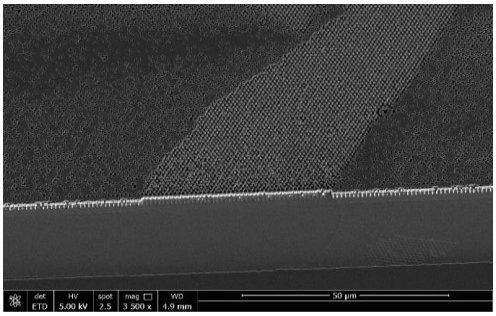

Figure 7 Newton Rings formation when sample observed under SEM, bright and dark fringes due to constructive and destructive interferences

The newton's rings problem can be lessened by removing the thick photoresist from the surface which is acting like a curved glass underneath the flat photomask. By eliminating the PR thickness, both photomask and the GaAs would be flat which will have a good contact at the center and the corners. This will reduce air gap difference between the two surfaces across the wafer.

Caution during dry etching is another important step to obtain the patterns on GaAs as etching for a longer time under RIE can disappear the patterns. Bringing down the pressure and power of RIE can help resolve this issue.

4. RESULTS

The fabricated wafer was observed under the SEM to carefully examine the shapes and depth of the structures. The squares and hexagons shapes obtained have round edges at the corners as seen in the figures below. The feature size and gap of the patterns obtained were measured using the SEM calibrated scale and correlate with the design parameters discussed in section 2. Figure 8 and 9 shows the SEM pictures of hexagons and squares pattern on GaAs. As observed, for the patterns with gap of 300nm between the neighboring squares or hexagons, inverse images were obtained while SEM pictures shows the positive produced patterns for the squares/hexagons of 400nm gap. [16]

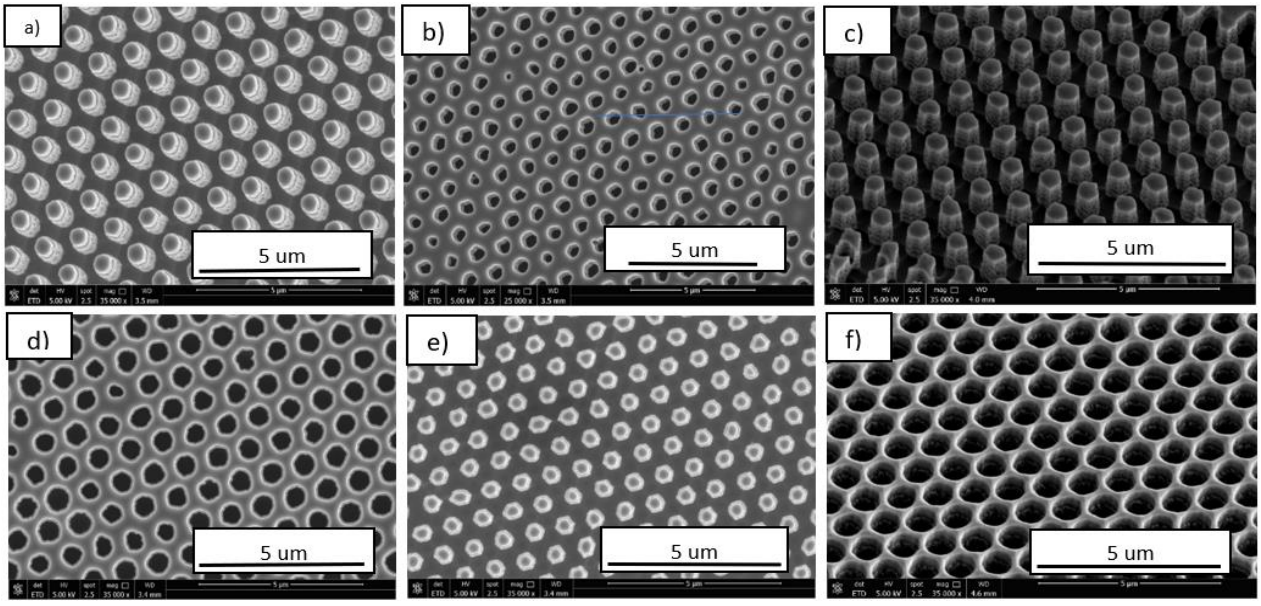

Figure 8 SEM results of Hexagons patterns on gallium arsenide for mid-IR antireflection texturing applications a) feature size 1.1um and gap 0.4um, b) feature size 1.1um and gap 0.3um, c) feature size 1.0um and gap 0.4um, d) feature size 1.0um and gap 0.3um, e) feature size 0.9um and gap 0.4um, f) feature size 0.9um and gap 0.3um,

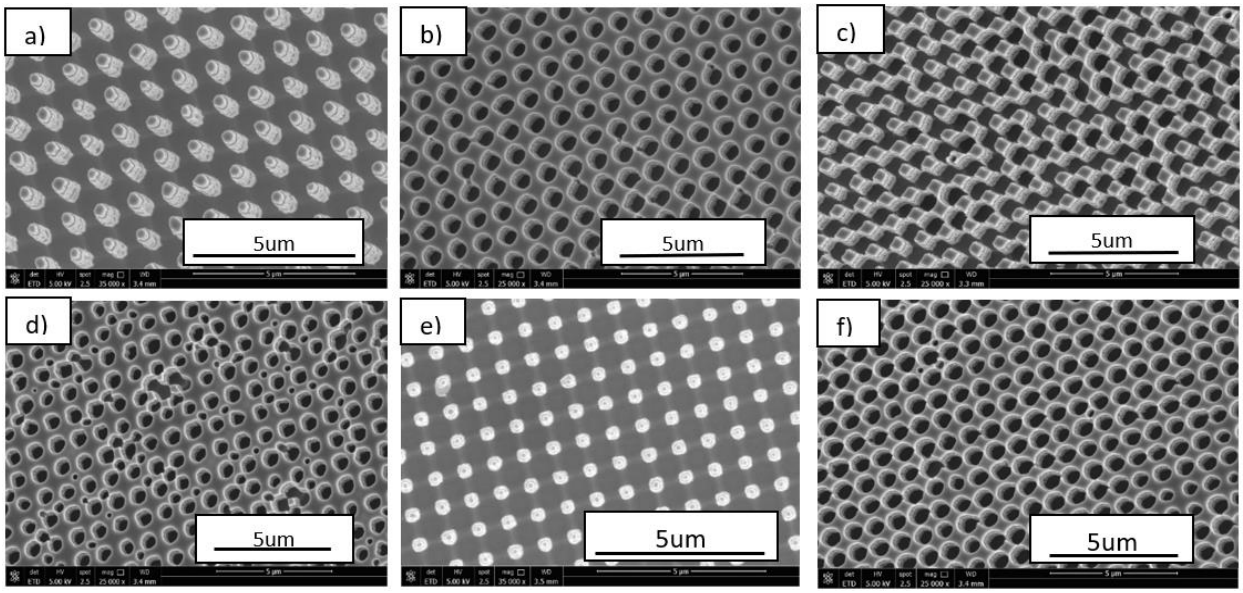

Figure 9 SEM results of Square patterns on gallium arsenide for mid-IR antireflection texturing applications a) feature size 1.1um and gap 0.4um, b) feature size 1.1um and gap 0.3um, c) feature size 1.0um and gap 0.4um, d) feature size 1.0um and gap 0.3um, e) feature size 0.9um and gap 0.4um, f) feature size 0.9um and gap 0.3um,

5. CONCLUSION

In this work, we briefly described the process to fabricate the nanostructures on gallium arsenide. The results from SEM shows the obtained pattern of squares and hexagons and design parameters were validated by comparing the SEM figures with the Photomask design.

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